THV6530

Boost converter / 2 channel charge pump

Description

THV6530 is a controller IC power supply system with boost converter and 2 channel charge pump circuit.
The positive and negative charge pumps provide regulated TFT LCD gate-on and gate-off supplies. The chip includes a VCOM buffer.
Soft start / Over current protection / Vout short circuit protection / Under voltage lock out protection / Thermal shut down are built in.
Mounted area is reducible by 16-pin QFN.

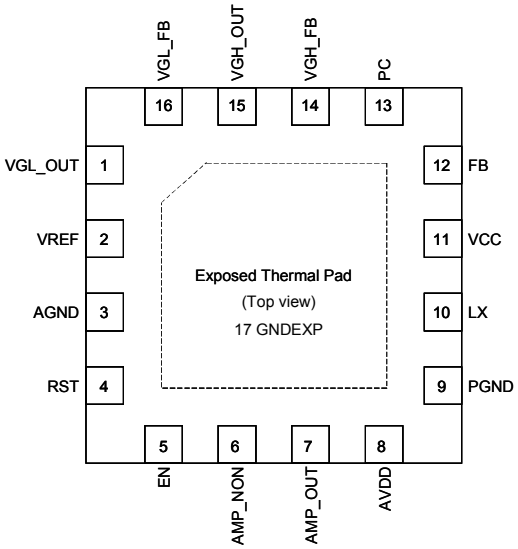
Application

・Mobile phone display
・Car Navigator display
・Laptop/Netbook/Tablet PC display

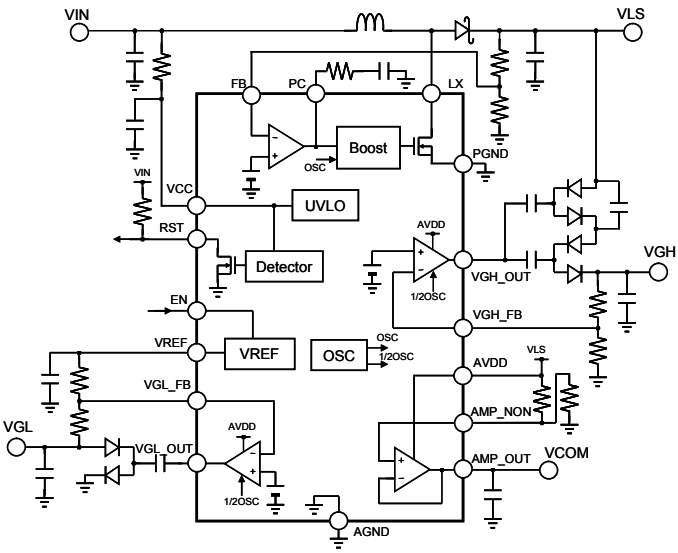
Features

・Input voltage range : 2.5V – 5.5V
・Boost converter
  Maximum output voltage : 16V
  Switching limit current : 1.4A
  Feedback voltage accuracy : +/-1%
  Switching frequency : 1.2MHz
・Positive charge pump
  Feedback voltage accuracy : +/-2%
  Switching frequency : 600kHz
・Negative charge pump
  Feedback voltage accuracy : +/-11%
  Switching frequency : 600kHz
・Buffer amplifier
  Output short-circuit current : +/-100mA
・Protection circuit
  Soft start
  Over current protection
  Under voltage lock out protection
  Thermal shut down
・3mm x 3mm QFN 16pin package

Pin Configuration



Block Diagram



Absolute Maximum Ratings

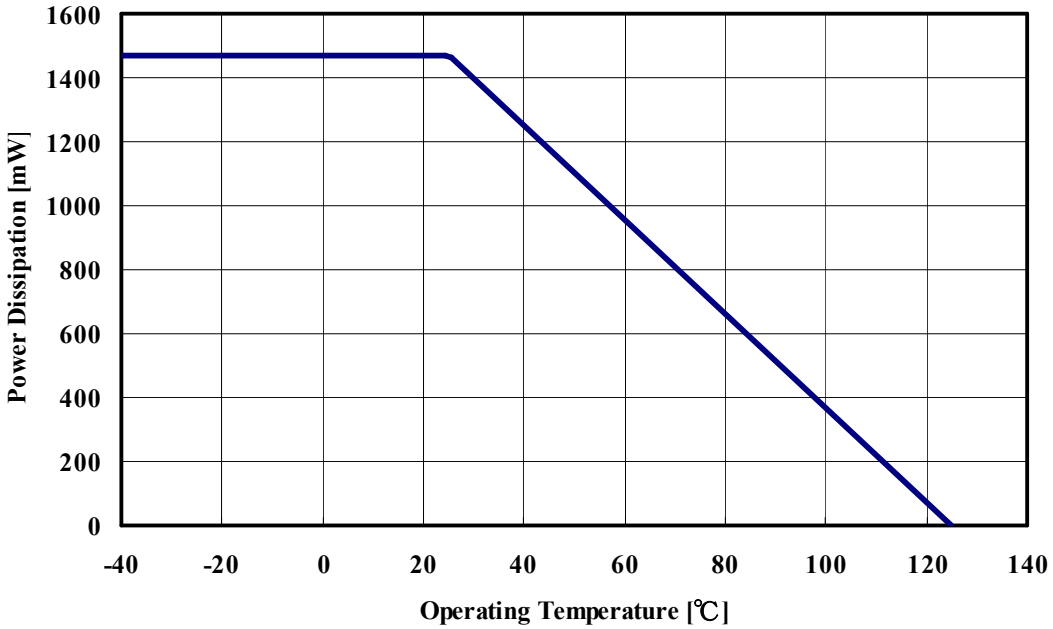
Parameter	Symbol	Rating	Units
VCC voltage	VCC	6.5	V
AVDD, LX voltage	VH	22	V
EN, RST voltage	VL	6.5	V
Power dissipation	Pd	1.47	W
Junction temperature (*1)	Tj	125	℃
Storage temperature range	Tstg	-55 to +150	℃

*1. The operating temperature range should perform a thermal design, after consulting the thermal characteristic. Please use it in the range which does not exceed junction temperature.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
VCC voltage	2.5	-	5.5	V
AVDD voltage	6	-	16	V

Power Dissipation



Pin Description

Number	Name	Function	Description
1	VGL_OUT	Negative charge pump output pin	This pin is output for negative charge pump.
2	VREF	Reference output voltage pin	This pin is reference voltage for negative charge pump. Please connect capacitor to GND for stable voltage.
3	AGND	Analog ground pin	Analog ground of PMIC
4	RST	Reset output pin	Voltage detector output. RST is an open-drain output.
5	EN	Enable pin	If low level voltage is impressed, PMIC is shutdown.
6	AMP_NON	Operational amplifier non-inverting input pin	This pin is the non-inverting input of operational amplifier.
7	AMP_OUT	Operational amplifier output pin	This pin is output of operational amplifier.
8	AVDD	Charge pump supply and operational amplifier supply pin	This pin is input supply for operational amplifier, positive charge pump.
9	PGND	Power ground pins	Power ground of boost converter.
10	LX	Boost converter switching output pin	This pin is switching output of boost converter.
11	VCC	Supply voltage pin	Power supply pin.
12	FB	Boost converter feedback voltage sense input pin	This pin is feedback input for boost converter.
13	PC	Boost converter error amplifier output pin	This pin is the boost converter error amplifier output. Please connect resistance and capacitor to GND for phase compensation.
14	VGH_FB	Positive charge pump feedback sense input pin	This pin is feedback input for positive charge pump.
15	VGH_OUT	Positive charge pump output pin	This pin is output for positive charge pump.
16	VGL_FB	Negative charge pump feedback sense input pin	This pin is feedback input for negative charge pump.
17	GND EXP	Back side	GND EXP should be soldered to GND to improve the thermal characteristics.

Electrical Characteristics （at VCC＝3.3V , AVDD=8.5V , Ta=25℃, unless otherwise noted）

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
System supply						
Input quiescent Current 1	Icc1	Vfb=1.35V(No switching)	-	0.3	-	mA
Input quiescent Current 2	Icc2	Vfb=1.15V(Switching)	-	0.8	-	mA
Reference voltage	Vref	Iref=-50uA	1.176	1.200	1.224	V
Reference Load Regulation voltage	dVref1	Iref=0uA to -100uA	-	1	5	mV
Reference Line Regulation voltage	dVref2	Iref=-100uA VCC=2.5V to 5.5V	-	2	5	mV
UVLO threshold voltage	Vuvlo	VCC rising	1.8	2.0	2.2	V
UVLO hysteresis voltage	Vuvloh		-	0.1	-	V
Short circuit delay time	Tscp		-	100	-	msec
EN threshold voltage	Venh		2	-	-	V
	Venl		-	-	0.8	V
Boost converter						
FB voltage	Vfb		1.188	1.200	1.212	V
FB input bias current	Ifb		-40	0	40	nA
Boost converter switching frequency	Fosc1		900	1200	1500	kHz
Boost converter maximum duty cycle	Dmax		85	90	94	%
LX ON-resistance	Ron1		-	700	-	mΩ
LX leakage current	Ileak	Vlx=16V	-	-	10	uA
LX current limit	Ilim		1.4	1.8	2	A
FB soft start	Tss1		-	7	-	msec
FB short circuit voltage	Vuvp1		-	0.95	-	V
Positive charge pump Regulator						
FBP voltage	Vfbp		1.176	1.200	1.224	V
FBP input bias current	Ifbp_bias		-40	0	40	nA
FBP switching frequency	Fosc2			1/2xFosc1		kHz
FBP high-side ON-resistance	Ron2h	Vavdd=10V	-	20	-	Ω
FBP low-side ON-resistance	Ron2l	Vavdd=10V	-	20	-	Ω
FBP soft start	Tss2		-	5	-	msec
FBP short circuit voltage	Vuvp2		-	0.95	-	V
Negative charge pump Regulator						
FBN voltage	Vfbn		0.210	0.240	0.270	V
FBN input bias current	Ifbn_bias		-40	0	40	nA
FBN Switching frequency	Fosc3			1/2xFosc1		kHz
FBN high-side ON-resistance	Ron3h	Vavdd=10V	-	20	-	Ω
FBN low-side ON-resistance	Ron3l	Vavdd=10V	-	20	-	Ω
FBN soft start	Tss3		-	5	-	msec
FBN short circuit voltage	Vuvp3		–	0.45	-	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Buffer amplifier						
AVDD quiescent Current	Iavdd		-	0.6	1.2	mA
Input offset voltage	Voff	Vamp_non=1/2AVDD	–15	0	15	mV
Input bias current	Iamp_non		-100	0	100	nA
Input common-mode voltage	Vamp_non		-0.3	-	AVDD+ 0.3V	V
Output high voltage	Vout_h	Iamp_out=5mA	AVDD- 0.2	-	-	V
Output low voltage	Vout_l	Iamp_out=-5mA	-	-	0.2	V
Slew rate	SR	Vamp_out=20% to 80% CL=10pF, RL=10kΩ	8	12	-	V/ usec
Short circuit high current	Iamp_h	Vamp_out=0V	100	150	-	mA
Short circuit low current	Iamp_l	Vamp_out=AVDD	100	150	-	mA
Reset						
Reset threshold voltage	Vrst		-	2.6	-	V
Reset hysteresis voltage	Vrsth		-	0.1	-	V
Reset output voltage	Vrst_o	Irst=1mA	-	-	0.4	V
Reset output delay time	Trst		-	120	-	msec

Function

Boost converter

The LCD panel VLS supply is generated from a high-efficiency PWM boost converter operating with current mode control, and the switching frequency is 1.2MHz. During the on-period, T_{ON}, the synchronous FET connects one end of the inductor to ground, therefore increasing the inductor current. After the FET turns off, the inductor switching node, LX, is charged to a positive voltage by the inductor current. The freewheeling diode turns on and the inductor current flows to the output capacitor.

The converter operates in continuous conduction mode when the load current I_{VLS} is at least one-half of the inductor ripple current ΔI_{rip}.

$$I_{IN} \geq \frac{\Delta I_{rip}}{2}$$

$$\Delta I_{rip} = \frac{(VLS - V_{IN}) \times V_{IN}}{L \times F_{OSC} \times VLS}$$

The output voltage (VLS) is determined by the duty cycle(D) of the power FET on-time and the input voltage, V_{IN}.

$$VLS = \frac{V_{IN}}{1 - D}$$

The average load current, I_{VLS}, can be calculated from the power conservation law.

$$\eta \times V_{IN} \times I_{IN} = VLS \times I_{VLS}$$

where η is the power conversion efficiency. For a lower load current, the inductor current would decay to zero during the free-wheeling period and the output node would be disconnected from the inductor for the remaining portion of the switching period. The converter would operate in the discontinuous conduction mode .

Current mode control is well known for its robustness and fast transient response. An inner current feedback loop sets the on-time and the duty cycle such that the current through the inductor equals to the current computed by the compensator. This loop acts within one switching cycle. A slope compensation ramp is added to suppress sub-harmonic oscillations. An outer voltage feedback loop subtracts the voltage on the FB pin from the internal reference voltage and feeds the difference to the compensator operational transconductance amplifier. This amplifier is compensated by an external R-C network to allow the user to optimize the transient response and loop stability for the specific application conditions.

The output voltage VLS can be set by external resistor divider R1 and R2 connected to FB.

$$VLS = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right)$$

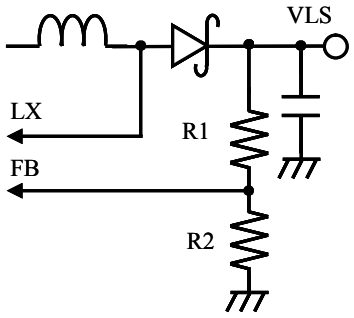


Fig. 1 FB setup

[Compensator selection]

This current mode boost converter has a current sense loop and a voltage feedback loop. The current sense loop does not need any compensation. The voltage feedback loop is compensated by an external series R-C network R_{PC} and C_{PC} from PC pin to ground. R_{COMP} is set to define the high frequency integrator gain for loop bandwidth which relates to the transient response. C_{PC} is set to ensure the loop stability.

[Output capacitor selection]

The output voltage ripple due to converter switching is

determined by the output capacitor total capacitance, C_{OUT}, and the output

$$VLS_{rip} = \frac{D \times I_{OUT}}{F_{OSC} \times C_{OUT}} + I_{peak} \times ESR$$

$$I_{peak} = I_{IN} + \frac{\Delta I_{rip}}{2}$$

The first ripple component can be reduced by increasing C_{OUT} since F_{OSC} is fixed 1.2MHz(typ). Changing C_{OUT} may require adjustment of compensation R and C in order to provide adequate phase margin and loop bandwidth.

The second ripple component can be reduced by selecting low-ESR ceramic capacitors and using several smaller capacitors in parallel instead of just one large capacitor.

[Inductor selection]

To prevent magnetic saturation of the inductor core the inductor has to be rated for a maximum current larger than I_{PK} in a given application. Since the chip provides current limit protection of 1.8A, it is generally recommended that the inductor be rated at least for 1.8A.

Selection of the inductor requires trade-off between the physical size (footprint x height) and its electrical properties (current rating, inductance, resistance). Within a given footprint and height, an inductor with larger inductance typically comes with lower current rating and often larger series resistance. Larger inductance typically requires more turns on the winding, a smaller core gap or a core material with a larger relative permeability. An inductor with a larger physical size has better electrical properties than a smaller inductor.

It is desirable to reduce the ripple current ΔI_{rip} in order to reduce voltage noise on the input and output capacitors. In practice, the inductor is often much larger than the capacitors and it is easier and cheaper to increase the size of the capacitors. The ripple current ΔI_{rip} is then chosen the largest possible while at the same time not degrading the maximum input and output current that the converter can operate with before reaching the current limit of the chip or the rated current of the inductor.

$$I_{peak} = I_{IN} + \frac{\Delta I_{rip}}{2} \le I_{MAX}$$

For example, ΔI_{rip} could be set to 20% of I_{MAX}

Voltage detector circuit

The internal voltage detector circuit monitors the chip ut voltage VIN. The chip can either drive RST pin low or leave it floating. While floating, RST is pulled high by an external pull up resistor. When VIN drops below 2.6V the chip pulls RST pin low. In order to release RST the VIN voltage must rise above 2.7V. The voltage detector circuit is disabled and RST is floating while the chip is disabled and for 120ms from the time the chip is enabled (VIN>UVLO and EN is high).

Positive charge pump (VGH)

The positive charge pump is used to generate the TFT LCD gate on voltage. The output voltage, VGH, can be set by an external resistive divider.

Voltage V_{VGH_FB} is typically 1.2V. A single stage charge pump can produce an output voltage less than approximately twice the charge pump input voltage VLS. The output voltage VGH is regulated as the following equation.

$$VGH = V_{VGH\_FB} \times \frac{R_5 + R_6}{R_5}$$

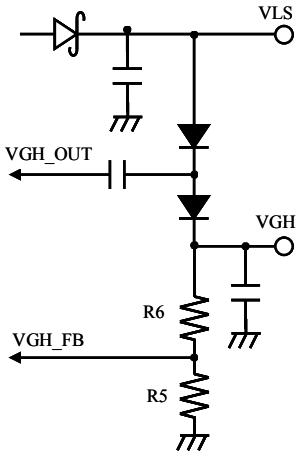


Fig. 2 VGH setup

Negative charge pump (VGL)

The negative charge pump is used to generate the TFT LCD gate off voltage. The output voltage, VGL, is set with an external resistive divider from its output to VREF with the midpoint connected to VGL_FB. The error amplifier compares the feedback signal from VGL_FB with an internal reference 240mV. The output voltage VGL is regulated as the following equation. The output voltage VGL is regulated as the following equation. VREF is 1.2V.

$$VGL = V_{VGL\_FB} - \frac{R_8}{R_7}(V_{VREF} - V_{VGL\_FB})$$

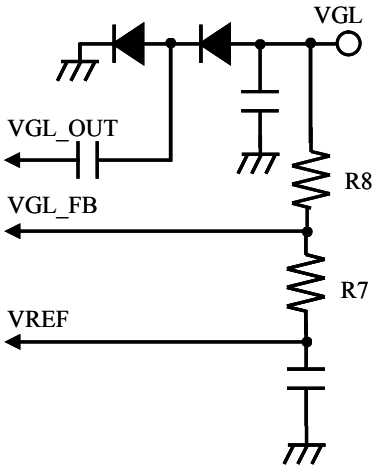


Fig. 3 VGL setup

VCOM buffer

The VCOM buffer generates the bias supply for the back plane of an LCD screen which is capacitively coupled to the pixel drive voltage. The purpose of the VCOM buffer is to hold the bias voltage steady while pixel voltage changes dynamically. The buffer is designed to sustain up to ±75mA of output current. In transients, it can deliver up to 150mA at which point the over current protection circuit limits the output current. Excessive current draw over a period of time may cause the chip temperature to rise and set off the over temperature protection circuit.

Protection circuits

Under voltage lock out protection (UVLO)

The UVLO function is carried in order to prevent malfunction in the state where input voltage is low. A boost converter is suspended to the power supply voltage which can carry out operational stability. UVLO is released by more than 1.8V input voltage. And a boost converter carries out, after starting soft start operation.

During normal operation (after completing the soft start sequence) THV6530 constantly monitors feedback pins FB, VGH_FB and VGL_FB. A fault condition occurs if FB falls below 0.95V or VGH_FB falls below 0.95V or VGL_FB rises above 0.45V. If any of the fault conditions persist for longer than 100ms, the chip sets a fault latch and shuts down. To turn the power supplies back on requires cycling of VIN supply below the UVLO level or toggling the EN pin low and high. This will clear the fault latch and restore normal operation.

Soft start (SS)

The boost converter carries the soft start function in order to prevent the rush current at a start-up. This function is to raise output voltage slowly. It is because overshooting and rush current occur when input voltage is inputted.

The soft-start time of the boost controller is 7ms, and the soft-start time of positive and negative charge pump is 5ms.

Over current protection (OCP)

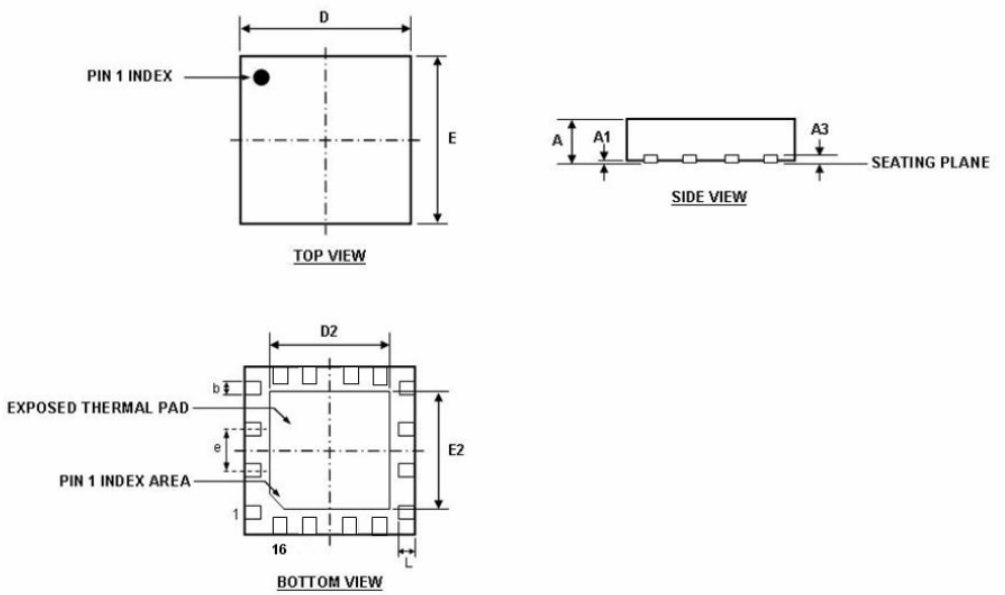
In order to restrict the over-current by the abnormalities of load, etc., the over-current protection circuit is built in. Over-current detection of pulse-by-pulse system is adopted. An output transistor is turned off if the current which flows into an output transistor reaches boost converter limit current (Ilim). An over-current protection circuit detects the peak current of an inductor. Input-and-output voltage and ripple current is taken into consideration.

Thermal shut down (TSD)

In order to prevent destruction by heat, the thermal shutdown circuit is built in. If the junction temperature Tj is 125°C or more, the thermal shutdown circuit will operate and it will stop switching operation. Moreover, the hysteresis of a thermal shutdown circuit is 15°C. If Tj falls, output voltage will return.

Package Dimensions

QFN 16-pin



DIMENSION	MIN (mm)	MAX (mm)
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.60	1.80
E	3.00 BSC	
E2	1.60	1.80
e	0.50 BSC	
L	0.30	0.45

Notes:
1) All dimensions are in millimeters.

Recommend connecting Back Exposed Pad with GND for a thermal characteristic improvement.

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
3. This material contains our copyright, know-how or other proprietary. Copying or disclosing to third parties the contents of this material without our prior permission is prohibited.
4. Note that if infringement of any third party's industrial ownership should occur by using this product, we will be exempted from the responsibility unless it directly relates to the production process or functions of the product.
5. This product is presumed to be used for general electric equipment, not for the applications which require very high reliability (including medical equipment directly concerning people's life, aerospace equipment, or nuclear control equipment). Also, when using this product for the equipment concerned with the control and safety of the transportation means, the traffic signal equipment, or various Types of safety equipment, please do it after applying appropriate measures to the product.
6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.
9. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

THine Electronics, Inc.
sales@thine.co.jp