THV6520

Boost converter / Charge pump

Description

THV6520 is a controller IC power supply system with boost converter and charge pump circuit.

The charge pump provide regulated TFT LCD gate-on and gate-off supplies. The chip includes a VCOM buffer and a gate slop circuit and LDO.

Soft start / Over current protection / Under voltage lock out protection / Thermal shut down are built in.

Mounted area is reducible by 24-pin QFN.

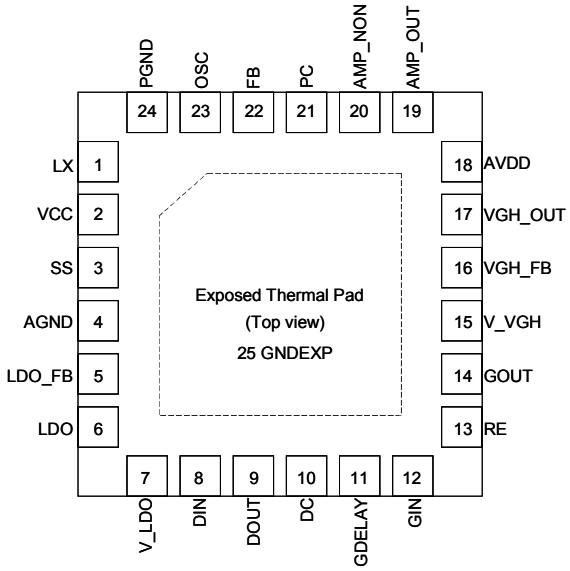
Application

・Mobile phone display
・Car Navigator display
・Laptop/Netbook/Tablet PC display

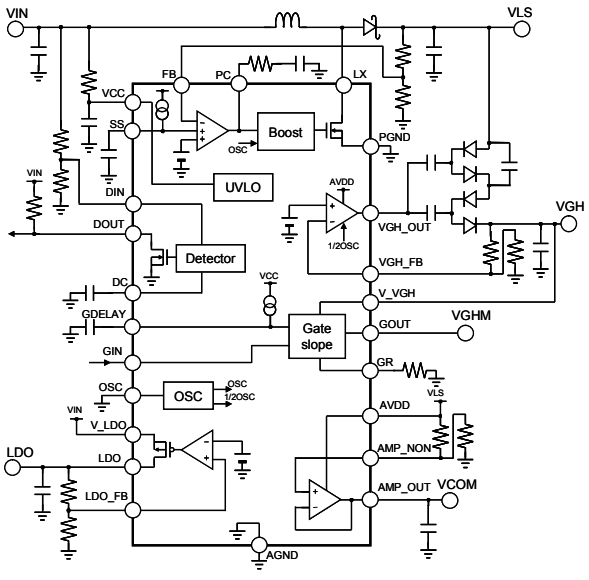
Features

・Input voltage range : 2.5V – 5.5V
・Boost converter
  Maximum output voltage : 16V
  Switching limit current : 2A
  Feedback voltage accuracy : +/-1%
  Switching frequency : 640kHz / 1.2MHz
・Charge pump
  Feedback voltage accuracy : +/-2%
  Switching frequency : 320kHz / 600kHz
・LDO
  Feedback voltage accuracy : +/-1.3%
  Output short-circuit current : 350mA
・Buffer amplifier
  Output short-circuit current : +/-90mA
・Gate slop
・Detector
・Protection circuit
  Soft start
  Over current protection
  Under voltage lock out protection
  Thermal shut down
・4mm x 4mm QFN 24pin package

Pin Configuration



Block Diagram



Absolute Maximum Ratings

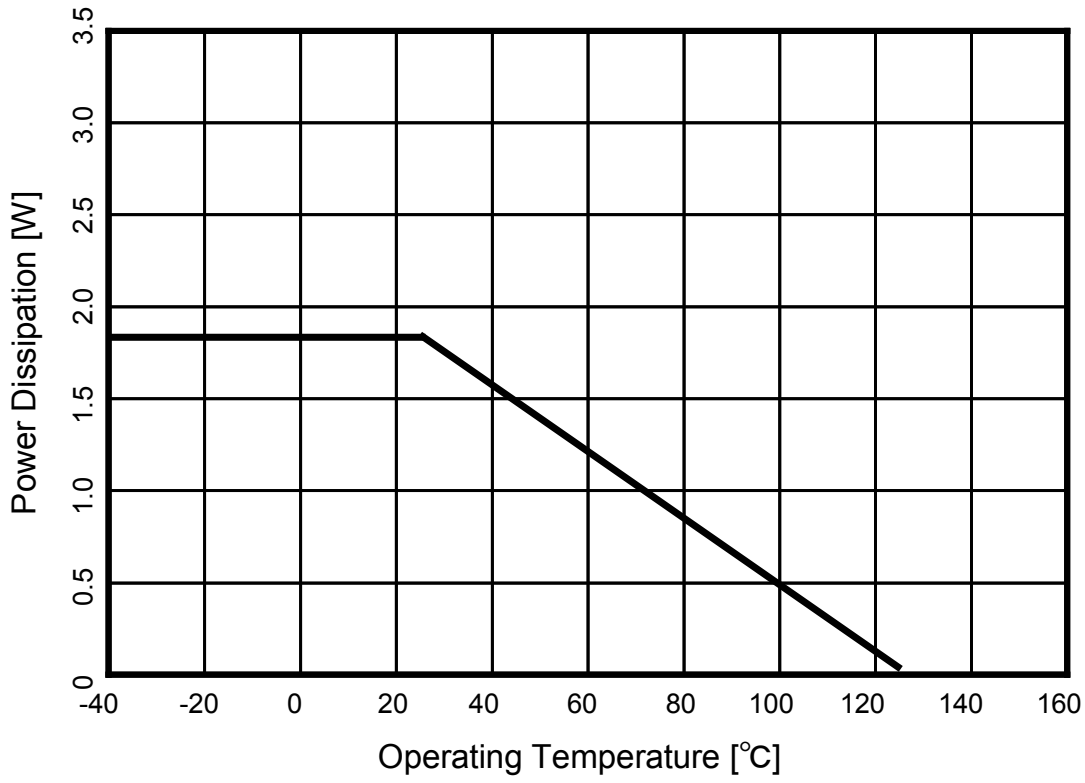
Parameter	Symbol	Rating	Units
VCC voltage	VCC	6.5	V
AVDD, LX voltage	VH1	22	V
V_VGH voltage	VH2	38	V
DOUT, DIN, VDIN, V_LDO voltage	VL	6.5	V
Power dissipation	Pd	1.8	W
Junction temperature (*1)	Tj	125	℃
Storage temperature range	Tstg	-55 to +150	℃

*1. The operating temperature range should perform a thermal design, after consulting the thermal characteristic. Please use it in the range which does not exceed junction temperature.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
VCC、V_LDO voltage	2.5	-	5.5	V
AVDD voltage	6	-	15	V

Power Dissipation



Pin Description

Number	Name	Function	Description
1	LX	Boost converter switching output pin	This pin is switching output of boost converter.
2	VCC	Supply voltage pin	Power supply pin
3	SS	Soft start set pin	This pin is set by soft start for boost converter. Please connect capacitor to GND for soft start time.
4	AGND	Analog ground pin	Analog ground of PMIC
5	LDO_FB	LDO feedback input pin	This pin is input for LDO feedback.
6	LDO	LDO output pin	This pin is output for LDO.
7	V_LDO	LDO supply voltage pin	This pin is input supply for LDO.
8	DIN	Detector input pin	This pin is input for detector.
9	DOUT	Detector output pin	This pin is output for detector. GIN is an open-drain output.
10	DC	Detector delay input pin	This pin is set by delay for detector. Please connect capacitor to GND for delay time.
11	GDELAY	Gate slop start delay input pin	This pin is set by delay for gate slop start time.
12	GIN	Gate slop input pin	This pin is input for gate slop timing.
13	RE	Gate slop set pin	This pin is controlled gate slop voltage by external resistance.
14	GOUT	Gate slop output pin	This pin is output for gate slop.
15	V_VGH	Supply voltage for gate slop pin	This pin is input supply for gate slop circuit.
16	VGH_FB	Positive charge pump feedback sense input pin	This pin is feedback input for positive charge pump.
17	VGH_OUT	Positive charge pump output pin	This pin is output for positive charge pump.
18	AVDD	Charge pump supply and operational amplifier supply pin	This pin is input supply for operational amplifier, positive charge pump.
19	AMP_OUT	Buffer amplifier output pin	This pin is output of operational amplifier.
20	AMP_NON	Buffer amplifier non-inverting input pin	This pin is the non-inverting input of operational amplifier.
21	PC	Boost converter error amplifier output pin	This pin is the boost converter error amplifier output. Please connect resistance and capacitor to GND for phase compensation.
22	FB	Boost converter feedback voltage sense input pin	This pin is feedback input for boost converter.
23	OSC	Oscillator set pin	Low level voltage is 640kHz, high level voltage is 1.2MHz.
24	PGND	Power ground pins	Power ground of boost converter.
25	GND EXP	Back side.	GND EXP should be soldered to GND to improve the thermal characteristics.

Electrical Characteristics (at VCC＝3.3V , Ta=25℃, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
System supply						
Input quiescent Current 1	Icc1	Vfb=1.35V(No switching)	-	0.5	1	mA
Input quiescent Current 2	Icc2	Vfb=1.1V(Switching)	-	2	4	mA
Standby current	Ist	Ven<0.8V	-	-	5	uA
UVLO threshold voltage	Vuvlo	Vcc rising	1.8	2.0	2.2	V
UVLO hysteresis voltage	Vuvloh		-	0.1	-	V
Boost converter						
FB voltage	Vfb		1.228	1.240	1.252	V
FB input bias current	Ifb		-40	0	40	nA
Boost converter switching frequency 1	Fosc1	Vosc<(0.3xVcc)	-	640	-	kHz
Boost converter switching frequency 2	Fosc2	Vosc>(0.7xVcc)	1000	1200	1500	kHz
Boost converter maximum duty cycle	Dmax		86	90	-	%
Oscillator pull down resistance	Rosc		-	250	-	kΩ
LX ON-resistance	Ron1		-	200	500	mΩ
LX current limit	Ilim		-	2.0	-	A
LX leakage current	Ileak	Vlx=16V	-	-	0.1	uA
Soft start charge current	Iss		-	4	-	uA
FB short circuit voltage	Vscp		–	1.05	-	V
FB short circuit delay time	Tscp		-	160	-	msec
Charge pump Regulator						
FBP voltage	Vfbp		1.216	1.240	1.264	V
FBP switching frequency	Fosc3		-	1/2xFosc1	-	kHz
FBP short circuit voltage	Vscp		–	1.05	-	V
FBP high-side ON-resistance	Ronh	Vavdd=12V	-	20	-	Ω
FBP low-side ON-resistance	Ronl	Vavdd=12V	-	20	-	Ω
FBP soft start	Iss		-	4	-	uA
Gate slop						
GIN input high voltage	Vginh		1.5	-	-	V
GIN input low voltage	Vginl		-	-	0.6	V
VGH to GOUT ON-resistance	Rgouth		-	30	-	Ω
GOUT to RE ON-resistance	Rgoutl		-	25	-	Ω
Delay set current	Igdelay		18	20	22	uA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Buffer amplifier						
AVDD quiescent Current	Iavdd		-	0.5	1.0	mA
Input offset voltage	Voff		-17	-	+17	mV
Input bias current	Iamp_non		-	1	50	nA
Input common-mode voltage	Vamp_non		0.5	-	AVDD-0.5V	V
Output high voltage	Vout_h	Iamp=75mA	-	AVDD-1.5	-	V
Output low voltage	Vout_l	Iamp=-75mA	-	1.5	-	V
Slew rate	SR		-	12	-	V/usec
Short circuit high current	Iamp_h	Vamp_out=0V	90	140	180	mA
Short circuit low current	Iamp_l	Vamp_out=AVDD	90	140	180	mA
LDO						
LDO quiescent Current	Iv_ldo		–	90	-	uA
LDO FB voltage	Vfb_ldo		1.224	1.240	1.256	V
LDO current limit	Ildo		350	500	-	mA
LDO dropout voltage	dVldo	Ildo=350mA	-	350	500	mV
LED load regulation	dVldo2	Ildo=1mA to 300mA	-	-	0.5	%
Detector						
Detector threshold voltage	Vdet		-	1.1	-	V
Detector hysteresis voltage	Vdeth		-	0.05	-	V
Detector ON-resistance	Rdet		-	50	-	Ω
Detector output delay time	Trst	DC=100nF	-	12	-	msec

Function

Boost converter

The LCD panel VLS supply is generated from a high-efficiency PWM boost converter operating with current mode control, and the switching frequency is selectable between 640kHz and 1.2MHz. During the on-period, T_{ON}, the synchronous FET connects one end of the inductor to ground, therefore increasing the inductor current. After the FET turns off, the inductor switching node, LX, is charged to a positive voltage by the inductor current. The freewheeling diode turns on and the inductor current flows to the output capacitor.

The converter operates in continuous conduction mode when the load current I_{VLS} is at least one-half of the inductor ripple current ΔI_{rip}.

$$I_{IN} \geq \frac{\Delta I_{rip}}{2}$$

$$\Delta I_{rip} = \frac{(VLS - V_{IN}) \times V_{IN}}{L \times F_{OSC} \times VLS}$$

The output voltage (VLS) is determined by the duty cycle(D) of the power FET on-time and the input voltage, V_{IN}.

$$VLS = \frac{V_{IN}}{1 - D}$$

The average load current, I_{VLS}, can be calculated from the power conservation law.

$$\eta \times V_{IN} \times I_{IN} = VLS \times I_{VLS}$$

where η is the power conversion efficiency. For a lower load current, the inductor current would decay to zero during the free-wheeling period and the output node would be disconnected from the inductor for the remaining portion of the switching period. The converter would operate in the discontinuous conduction mode .

Current mode control is well known for its robustness and fast transient response. An inner current feedback loop sets the on-time and the duty cycle such that the current through the inductor equals to the current computed by the compensator. This loop acts within one switching cycle. A slope compensation ramp is added to suppress sub-harmonic oscillations. An outer voltage feedback loop subtracts the voltage on the FB pin from the internal reference voltage and feeds the difference to the compensator operational transconductance amplifier. This amplifier is compensated by an external R-C network to allow the user to optimize the transient response and loop stability for the specific application conditions.

The output voltage VLS can be set by external resistor divider R1and R2 connected to FB.

$$VLS = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right)$$

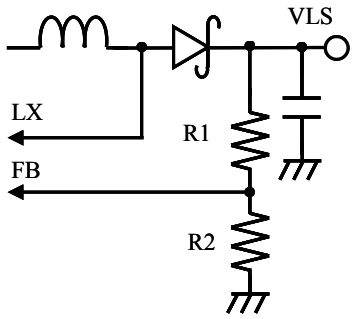


Fig. 1 FB setup

[Compensator selection]

This current mode boost converter has a current sense loop and a voltage feedback loop. The current sense loop does not need any compensation. The voltage feedback loop is compensated by an external series R-C network R_{PC} and C_{PC} from PC pin to ground. R_{COMP} is set to define the high frequency integrator gain for loop bandwidth which relates to the transient response. C_{PC} is set to ensure the loop stability.

[Output capacitor selection]

The output voltage ripple due to converter switching is

determined by the output capacitor total capacitance, C_{OUT}, and the output

$$VLS_{rip} = \frac{D \times I_{OUT}}{F_{OSC} \times C_{OUT}} + I_{peak} \times ESR$$

$$I_{peak} = I_{IN} + \frac{\Delta I_{rip}}{2}$$

The first ripple component can be reduced by increasing C_{OUT}. Changing C_{OUT} may require adjustment of compensation R and C in order to provide adequate phase margin and loop bandwidth.

The second ripple component can be reduced by selecting low-ESR ceramic capacitors and using several smaller capacitors in parallel instead of just one large capacitor.

[Inductor selection]

To prevent magnetic saturation of the inductor core the inductor has to be rated for a maximum current larger than I_{PK} in a given application. Since the chip provides current limit protection of 2A, it is generally recommended that the inductor be rated at least for 2A.

Selection of the inductor requires trade-off between the physical size (footprint x height) and its electrical properties (current rating, inductance, resistance). Within a given footprint and height, an inductor with larger inductance typically comes with lower current rating and often larger series resistance. Larger inductance typically requires more turns on the winding, a smaller core gap or a core material with a larger relative permeability. An inductor with a larger physical size has better electrical properties than a smaller inductor.

It is desirable to reduce the ripple current ΔI_{rip} in order to reduce voltage noise on the input and output capacitors. In practice, the inductor is often much larger than the capacitors and it is easier and cheaper to increase the size of the capacitors. The ripple current ΔI_{rip} is then chosen the largest possible while at the same time not degrading the maximum input and output current that the converter can operate with before reaching the current limit of the chip or the rated current of the inductor.

$$I_{peak} = I_{IN} + \frac{\Delta I_{rip}}{2} \le I_{MAX}$$

For example, ΔI_{rip} could be set to 20% of I_{MAX}

Voltage detector circuit

Voltage detector circuit senses the voltage on VDIN pin and turns on a pull-down FET that drives DOUT low if VDIN voltage falls below the applicable threshold level VDIN. When VDIN is rising, initially DOUT is pulled low. As soon as VDIN exceeds (V_{DIN} +ΔV_{DIN}), the reset timer is started. Once VDIN has remained above (V_{DIN} +ΔV_{DIN}) for at least T_D, the pull down FET opens and DOUT is driven high by an external pull-up resistor. During shut down, when VDIN falls below VDIN the pull down FET turns on and drives DOUT pin low. To the external voltage V_{ext}, the rising and falling detection thresholds $V_{DET,High}$ and $V_{DET,Low}$, respectively are set by the external voltage divider R3, R4.

$$V_{Det,High} = \frac{R_4 + R_3}{R_3}(V_{Din} + \Delta V_{Din})$$

$$V_{Det,Low} = \frac{R_4 + R_3}{R_3} V_{Din}$$

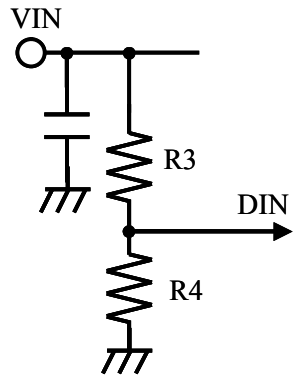


Fig. 2 Detector setup

The delay time is programmable by an external capacitor as equation. For example, setting DC = 100nF can generate around 12ms delay for reset signal.

T_D = 120K x DC.

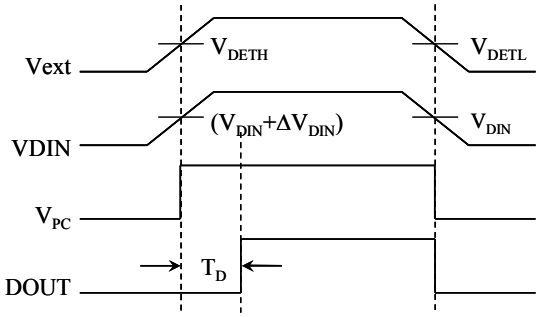


Fig. 3 Detector timing chart

Positive charge pump (VGH)

The positive charge pump is used to generate the TFT LCD gate on voltage. The output voltage, VGH, can be set by an external resistive divider.

Voltage V_{VGH_FB} is typically 1.24V. A single stage charge pump can produce an output voltage less than approximately twice the charge pump input voltage VLS. The charge pump can deliver up to 20mA of current. The maximum voltage VGH should not exceed 38V if it is used to supply the Gate slope circuit. The output voltage VGH is regulated as the following equation.

$$VGH = V_{VGH\_FB} \times \frac{R_5 + R_6}{R_5}$$

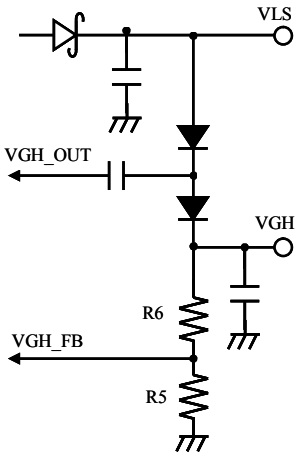


Fig. 4 VGH setup

Gate slope

The Gate slope is a flicker compensation circuit to reduce the coupling effect of gate lines, and is controlled by timing controller to modulate GOUT, the Gate-On voltage. This block is not activated until the below 3 conditions are satisfied: 1) The input voltage exceeds its UVLO, 2) No fault condition is detected, and 3) GDELAY exceeds its turn-on threshold. Once Gate slope activates and GIN is high, the internal switch between V_VGH and GOUT turns on and the switch between GOUT and GR turns off. If GIN is low, the internal switch between V_VGH and GOUT turns off and the switch between GOUT and GR turns on. At that time, the falling time and delay time of the Gate-On voltage are programmable by an external resistor connected between GR and GND.

VCOM buffer

The VCOM buffer generates the bias supply for the back plane of an LCD screen which is capacitively coupled to the pixel drive voltage. The purpose of the VCOM buffer is to hold the bias voltage steady while pixel voltage changes dynamically. The buffer is designed to sustain

up to ±75mA of output current. In transients, it can deliver up to 150mA at which point the over current protection circuit limits the output current. Excessive current draw over a period of time may cause the chip temperature to rise and set off the over temperature protection circuit.

LDO

The THV6520 has a integrated LDO which can supply up to 350mA current while the input voltage is 3.3V. It is suitable for the supply voltage to timing controller and source IC.

Protection circuits

Under voltage lock out protection (UVLO)

The UVLO function is carried in order to prevent malfunction in the state where input voltage is low. A boost converter is suspended to the power supply voltage which can carry out operational stability. UVLO is released by more than 1.8V input voltage. And a boost converter carries out, after starting soft start operation.

During steady-state operation, if the output of the boost converter is under 85% of the nominal value, the THL6520 activates an internal fault timer. If any condition indicates a continuous fault for the fault timer duration (160ms typ), the IC sets the fault latch to shut down all its output. Once the fault condition is removed, cycle the VIN (below the UVLO falling threshold) to clear the fault latch and reactivate the device. The fault-detection circuit is disabled during the soft-start ramp.

Soft start (SS)

The boost converter carries the soft start function in order to prevent the rush current at a start-up. This function is to raise output voltage slowly. It is because overshooting and rush current occur when input voltage is inputted. When power is turned on, an internal 4μA current source charges an external capacitor connected as SS. When power is turned off, the external capacitor will be discharged for the next soft start cycle.

Over voltage protection (OVP)

Over voltage protection is built in. If VLS is disconnecting, the output voltage of a boost converter is stopped and destruction of IC is prevented.

Over current protection (OCP)

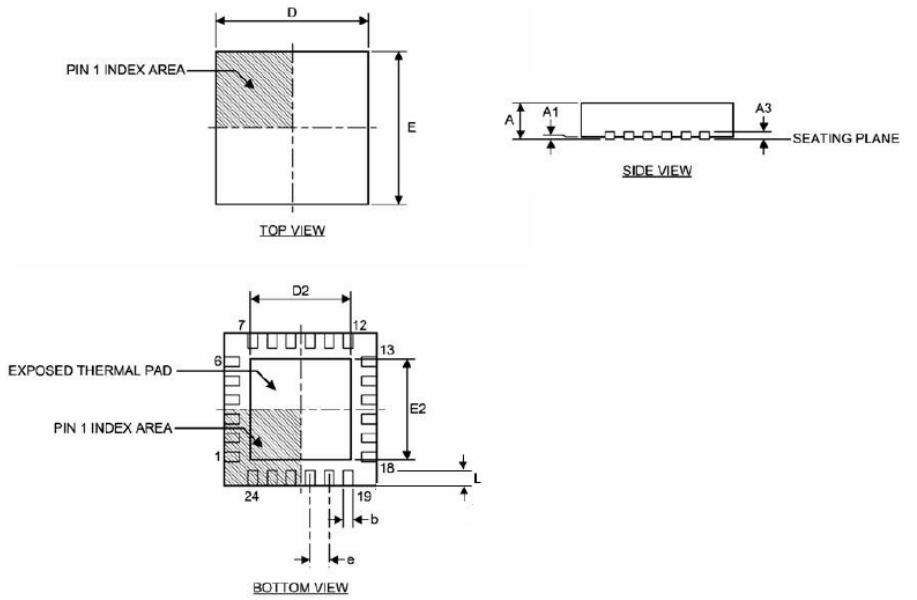
In order to restrict the over-current by the abnormalities of load, etc., the over-current protection circuit is built in. Over-current detection of pulse-by-pulse system is adopted. An output transistor is turned off if the current which flows into an output transistor reaches boost converter limit current (Ilim). An over-current protection circuit detects the peak current of an inductor. Input-and-output voltage and ripple current is taken into consideration.

Thermal shut down (TSD)

In order to prevent destruction by heat, the thermal shutdown circuit is built in. If the junction temperature Tj is 150°C or more, the thermal shutdown circuit will operate and it will stop switching operation. Moreover, the hysteresis of a thermal shutdown circuit is 15°C. If Tj falls, output voltage will return.

Package Dimensions

QFN 24-pin



DIMENSION	MIN (mm)	MAX (mm)
A	0.80	1.00
A1	0	0.05
A3	0.20 REF	
b	0.18	0.30
D	4.00 BSC	
D2	2.40	2.75
E	4.00 BSC	
E2	2.40	2.75
e	0.50 BSC	
L	0.35	0.45

Notes:
1) All dimensions are in millimeters.
2) Dimensions comply with JEDEC MO-220K, VGGD-6.

Recommend connecting Back Exposed Pad with GND for a thermal characteristic improvement.

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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