Application Note	*THAN0063_Rev.1.10_E*

THC63LVD1023B/THC63LVD1024 Application Note

Mode setting, System Diagram and PCB Design Guide

Date	Revision	Contents
2007/09/07	Rev.1.00_E	New created
2007/10/15	Rev.1.01_E	Typo
2008/08/06	Rev.1.10_E	Add Some figures

Contents

1. Mode Setting

THC63LVD1023B

			ASYNC	MODE3	MODE2	MODE1	MODE0
SYNC /ASYNC	Input/Output	Option	SYNC/ASYNC Select	Single In / Dual Out Input Port	Function select	Input mode	Output mode
			H: ASYNC L: SYNC	H: Data Port1 L: Data Port2	-	H: Single L: Dual	H: Single L: Dual
SYNC	Single In/ Single Out	Distribution off (Fig.2-1, 4-1)	L	*	L	H	H
		Distribution on (Fig.2-2)	L	*	H	H	H
	Single In/ Dual Out	DDR off, Port SW off (Use Data Port1) (Fig.2-3)	L	H or Open	L	H	L
		DDR on, Port SW off (Use Data Port1) (Fig.2-4)	L	H or Open	H	H	L
		DDR off, Port SW on (Use Data Port2) (Fig.2-5)	L	L	L	H	L
		DDR on, Port SW on (Use Data Port2) (Fig.2-6, 4-4)	L	L	H	H	L
	Dual In/ Single Out	- (Fig.2-7, 4-2)	L	*	*	L	H
	Dual In/ Dual Out	- (Fig.2-8)	L	*	*	L	L
ASYNC	Dual In/ Dual Out	Crosspoint SW off (Fig.2-9)	H	*	L	*	*
		Crosspoint SW on (Fig.2-10)	H	*	H	*	*

*: Don't care

THC63LVD1024

		MODE2	MODE1	MODE0
Input/Output	Option	DDR	Input mode	Output mode
		H: DDR on L: DDR off	H: Single L: Dual	H: Single L: Dual
Single In/Single Out (Fig.2-11, 4-1)	--	L	H	H
Single In/Dual Out (Fig.2-12, 4-2)	--	L	H	L
Dual In/Single Out (Fig.2-13/14, 4-4)	DDR off	L	L	H
	DDR on	H	L	H
Dual In/Dual Out (Fig.2-15, 4-5)	--	L	L	L

2. Signal Flow for Each Setting

THC63LVD1023B

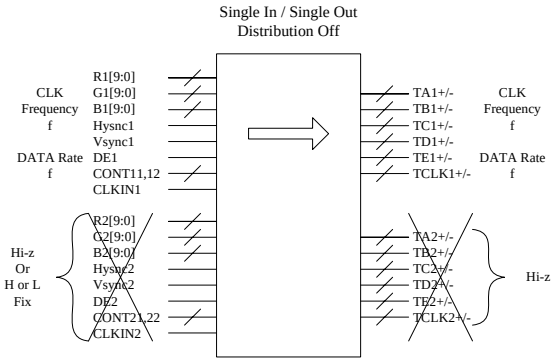


Fig2-1

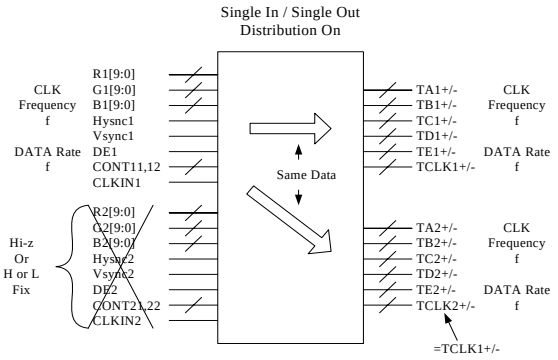


Fig2-2

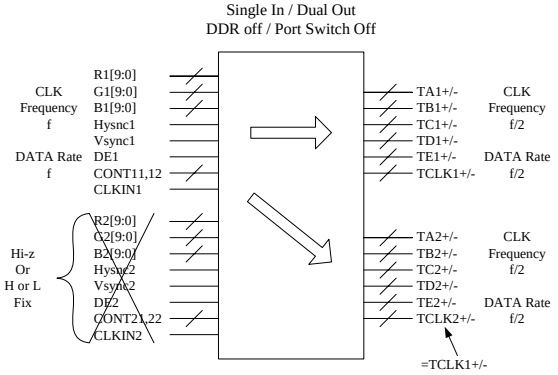


Fig2-3

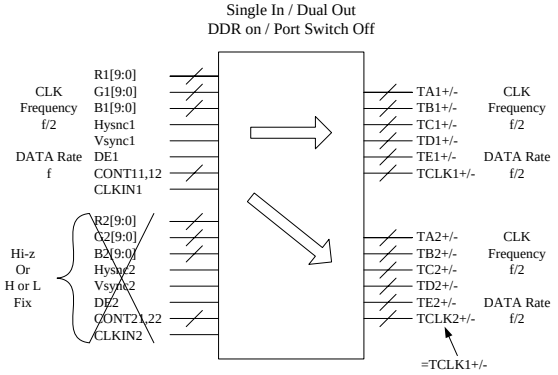


Fig2-4

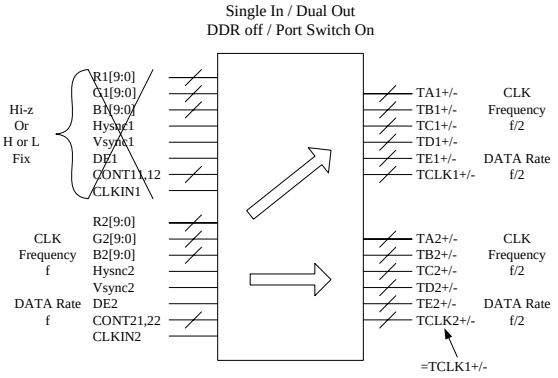


Fig2-5

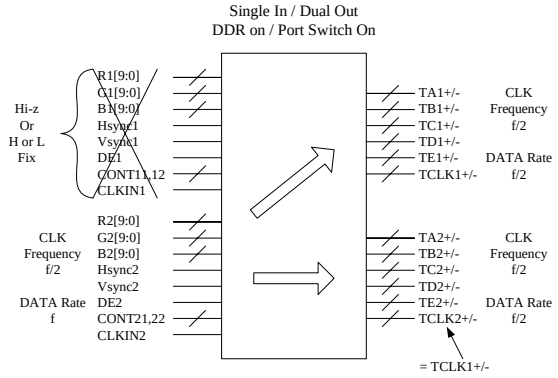


Fig2-6

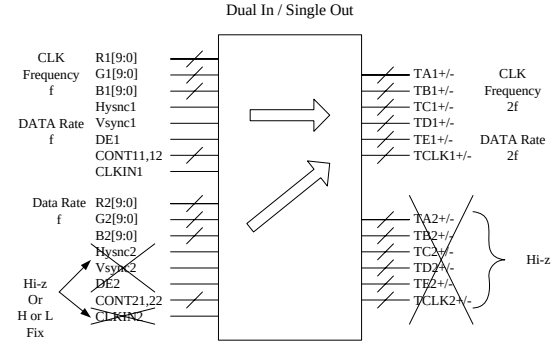


Fig2-7

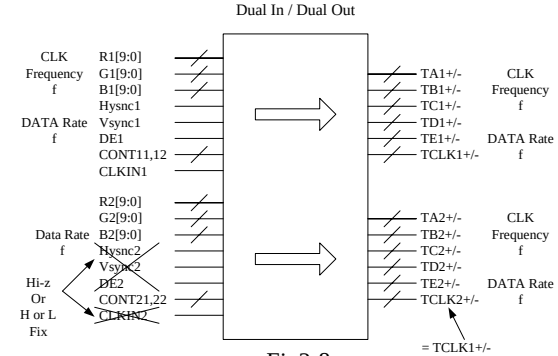


Fig2-8

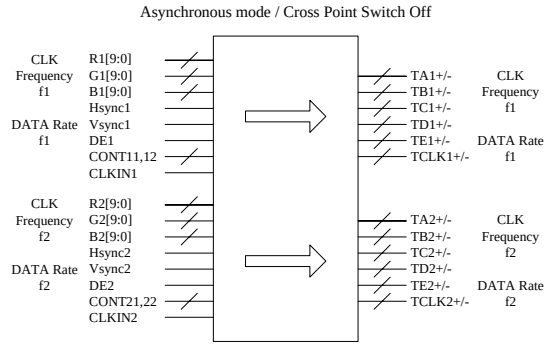


Fig2-9

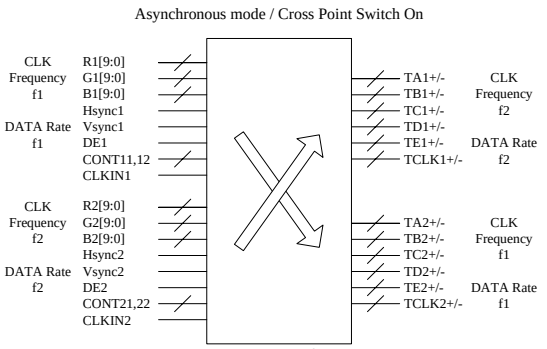


Fig2-10

THC63LVD1024

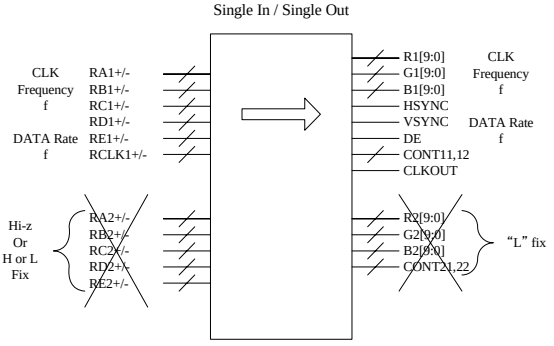


Fig2-11

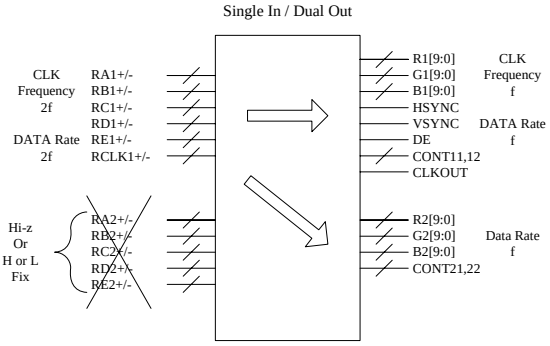


Fig2-12

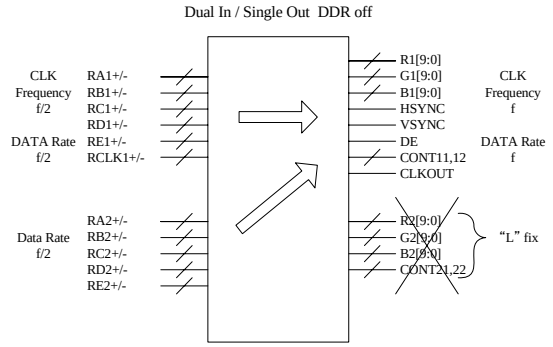


Fig2-13

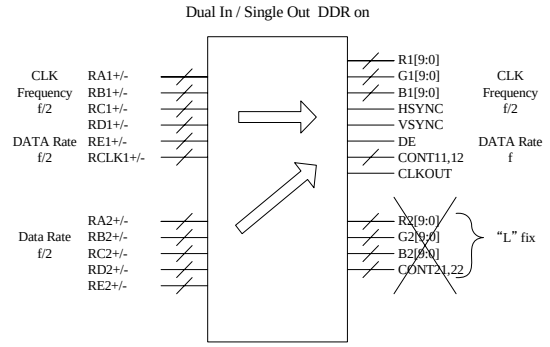


Fig2-14

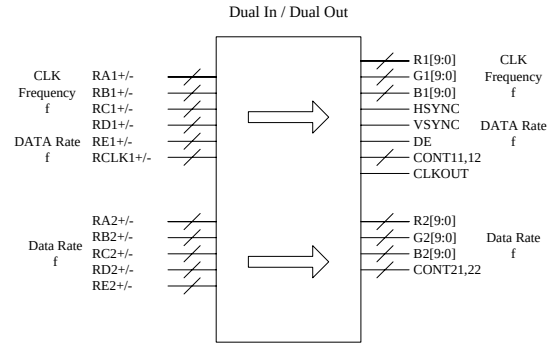
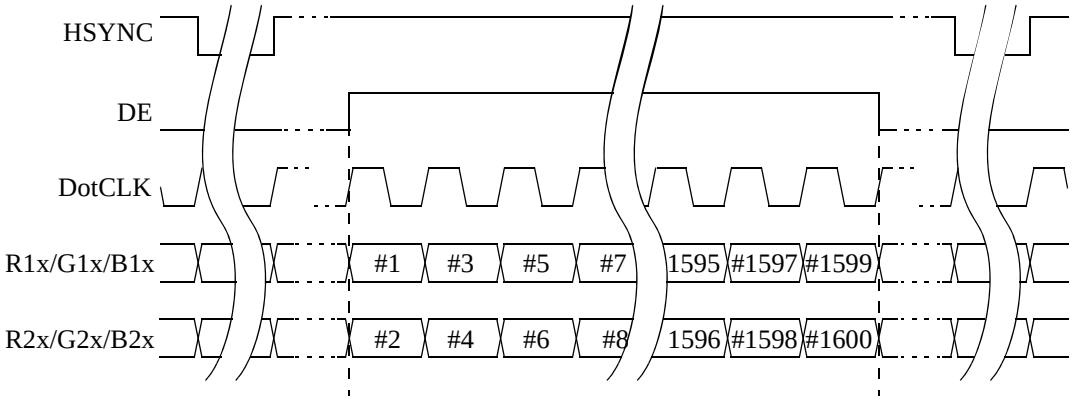
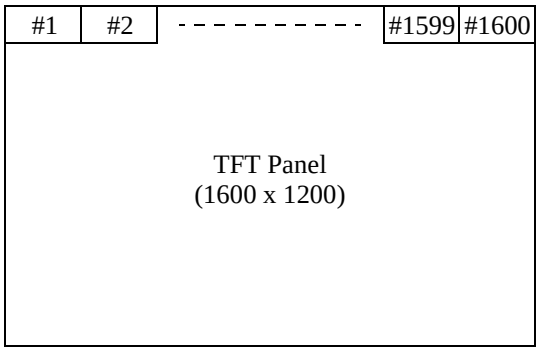


Fig2-15

3. TTL DATA Timing Diagram

Following are THC63LVD1023B TTL data input timing example for UXGA(1600 x 1200).





Note:

	R1x	G1x	B1x	R2x	G2x	B2x
MSB	R19	G19	B19	R29	G29	B29
	R18	G18	B18	R28	G28	B28
	R17	G17	B17	R27	G27	B27
	R16	G16	B16	R26	G26	B26
	R15	G15	B15	R25	G25	B25
	R14	G14	B14	R24	G24	B24
	R13	G13	B13	R23	G23	B23
	R12	G12	B12	R22	G22	B22
	R11	G11	B11	R21	G21	B21
LSB	R10	G10	B10	R20	G20	B20

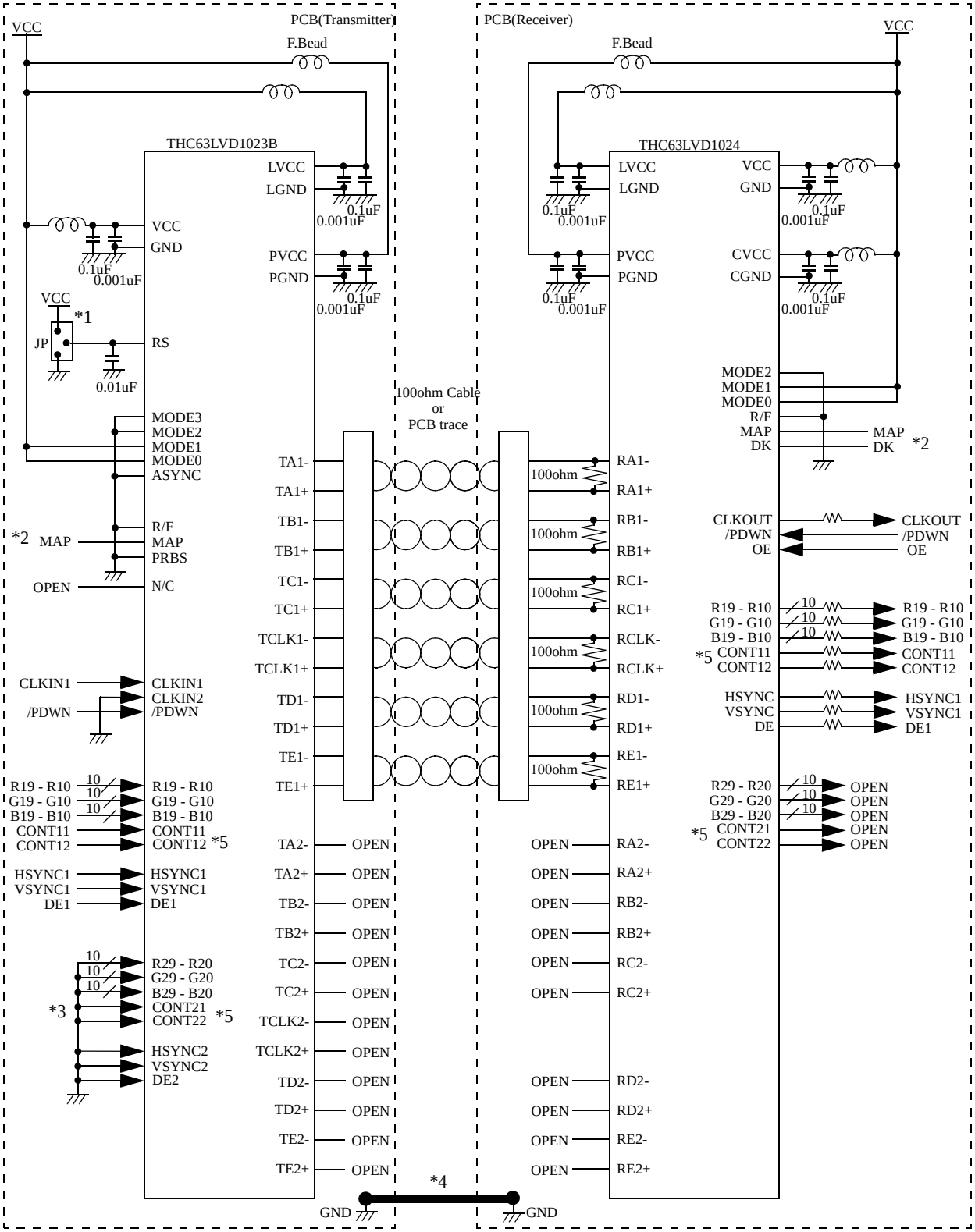
4. Example of System Diagram

1) Single Link(TTL/CMOS Input: 20~135MHz)

Example :

THC63LVD1023B : Falling edge / 10bit / Single in(TTL)-Single out(LVDS) / Distribution Off

THC63LVD1024 : Falling edge / 10bit / Single in(LVDS)-Single out(TTL)



*1 : If RS pin tied to VCC, LVDS swing is 350mV.
If RS pin tied to GND, LVDS swing is 200mV.

*2: Refer to datasheet

*3: L/H fix or Hi-z

*4: Connect each PCB GND

*5: CONT## pins can be used as data.

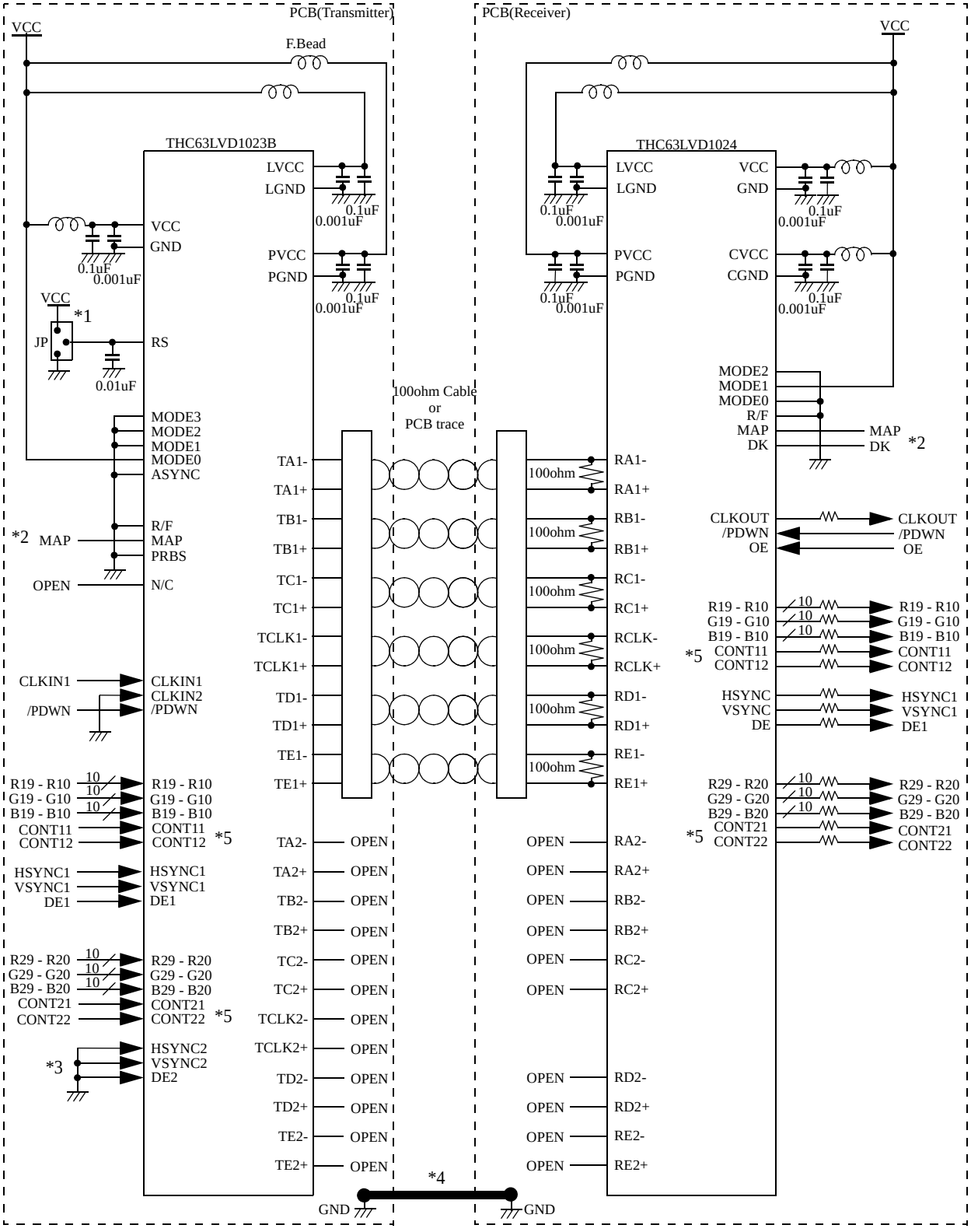
Fig. 4-1

2) Single Link (TTL/CMOS Input: 10~67.5MHz)

Example :

THC63LVD1023B : Falling edge / 10bit / Dual in(TTL)-Single out(LVDS)

THC63LVD1024 : Falling edge / 10bit / Single in(LVDS)-Dual out(TTL)



*1 : If RS pin tied to VCC, LVDS swing is 350mV.
If RS pin tied to GND, LVDS swing is 200mV.

*2: Refer to datasheet

*3: L/H fix or Hi-z

*4: Connect each PCB GND

*5: CONT## pins can be used as data

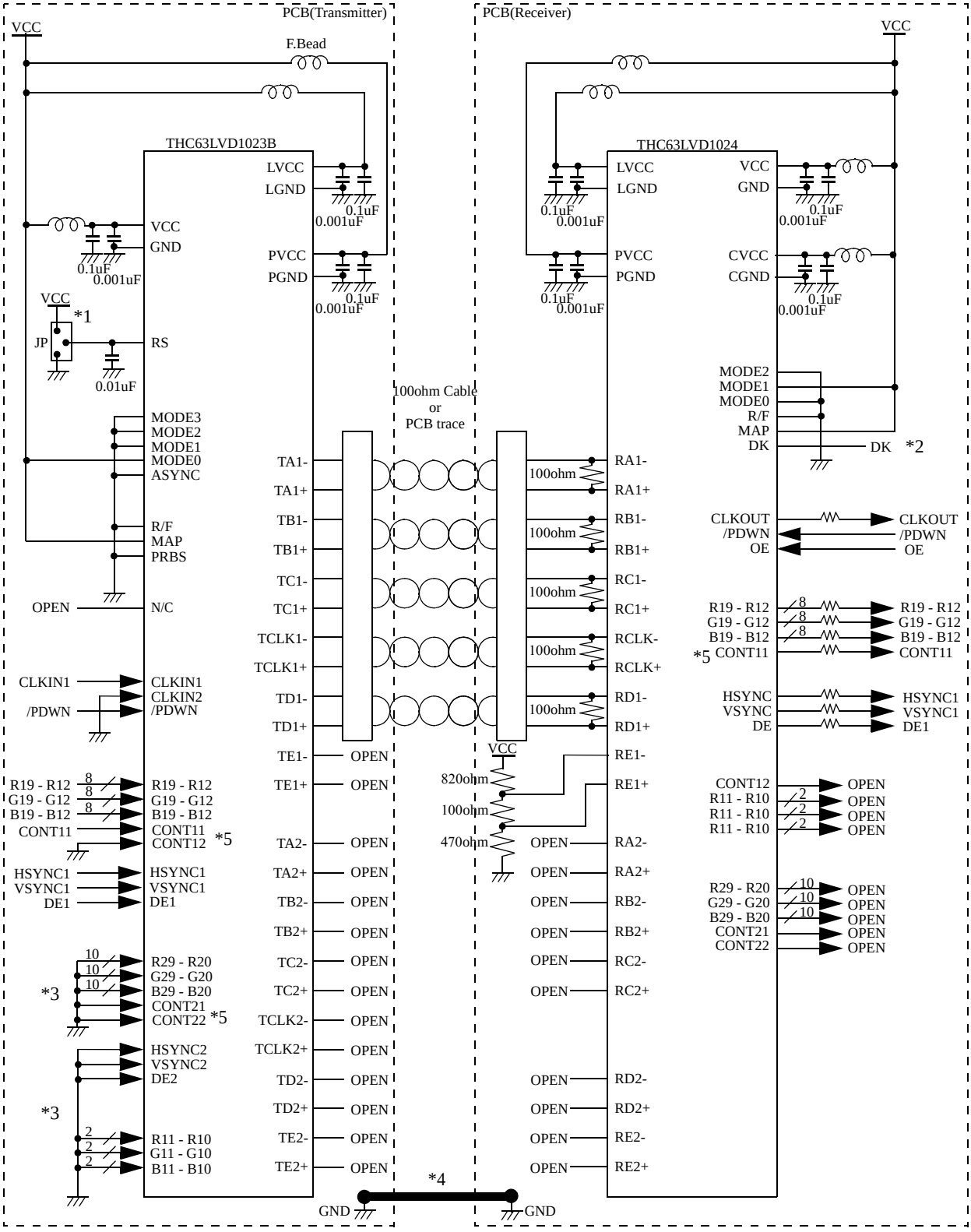
Fig. 4-2

3) Single Link (TTL/CMOS Input: 20~135MHz)

Example :

THC63LVD1023B : Falling edge / 8bit / Dual in(TTL)-Single out(LVDS)

THC63LVD1024 : Falling edge / 8bit / Single in(LVDS)-Dual out(TTL)



*1 : If RS pin tied to VCC, LVDS swing is 350mV.
If RS pin tied to GND, LVDS swing is 200mV.

*2: Refer to datasheet

*3: L/H fix or Hi-z

*4: Connect each PCB GND

*5: CONT## pins can be used as data

Fig. 4-3

4) Dual Link (TTL/CMOS Input:40~150MHz(DDR off),20~75MHz(DDR on))

Example :
THC63LVD1023B : Falling edge/ 10bit / Single in(TTL)-Dual out(LVDS) / DDR Off or On / Port Swtich On
THC63LVD1024 : Falling edge / 10bit / Dual in(LVDS)-Dual out(TTL) or Single Out / DDR Off or On

Note1: tDEINT = tTCIP*2n (n=integer)
Note2: tDEINT >= 4*tTCIP
Note3: tDEH >= 2k*tTCIP, tDEL >= 2m*tTCIP (k,m = integer)
(tDEINT = DE Period, tTCIP = CLKIN Period, tDEH = DE High Time, tDEL = DE Low Time) *2

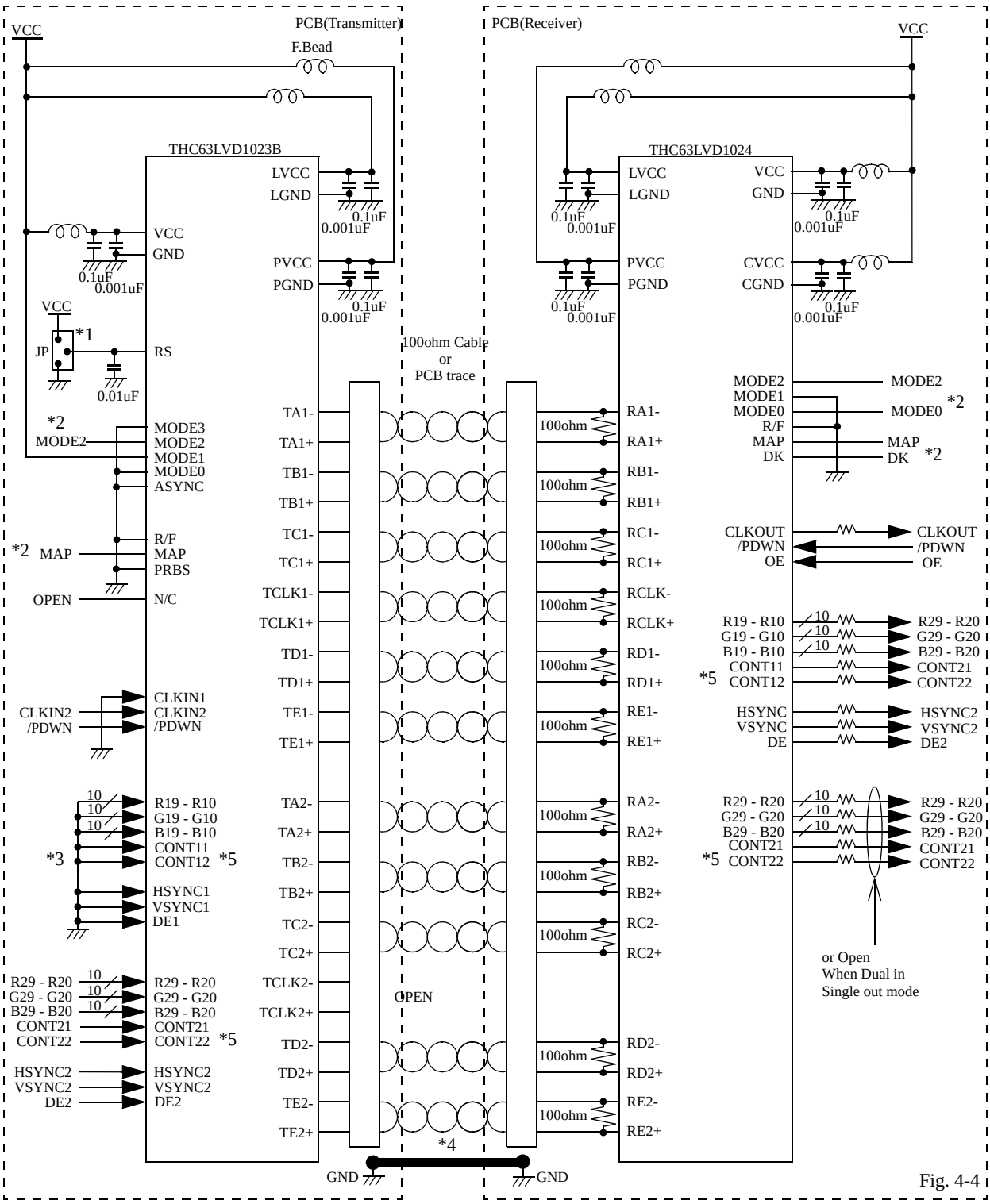


Fig. 4-4

*1 : If RS pin tied to VCC, LVDS swing is 350mV.
If RS pin tied to GND, LVDS swing is 200mV.

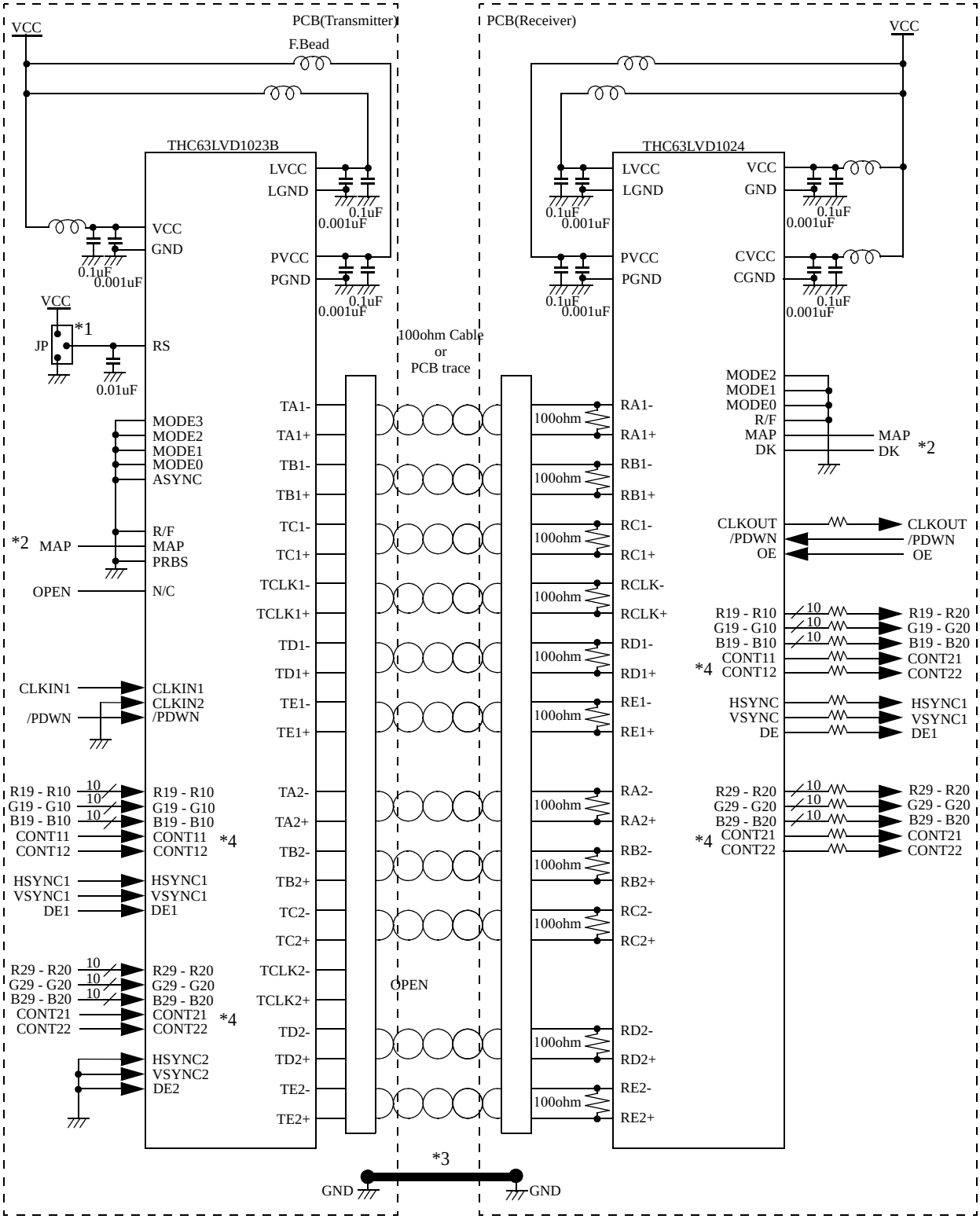
*2: Refer to datasheet
*3: L/H fix or Hi-z
*4: Connect each PCB GND
*5: CONT## pins can be used as data

5) Dual Link (TTL/CMOS Input: 20~135MHz)

Example :

THC63LVD1023B: Falling edge / 10bit / Dual in(TTL)-Dual out(LVDS)

THC63LVD1024 : Falling edge / 10bit / Dual in(LVDS)-Dual out(TTL)



*1 : If RS pin tied to VCC, LVDS swing is 350mV.
If RS pin tied to GND, LVDS swing is 200mV.

*2: Refer to datasheet

*3: Connect each PCB GND

*4: CONT## pins can be used as data

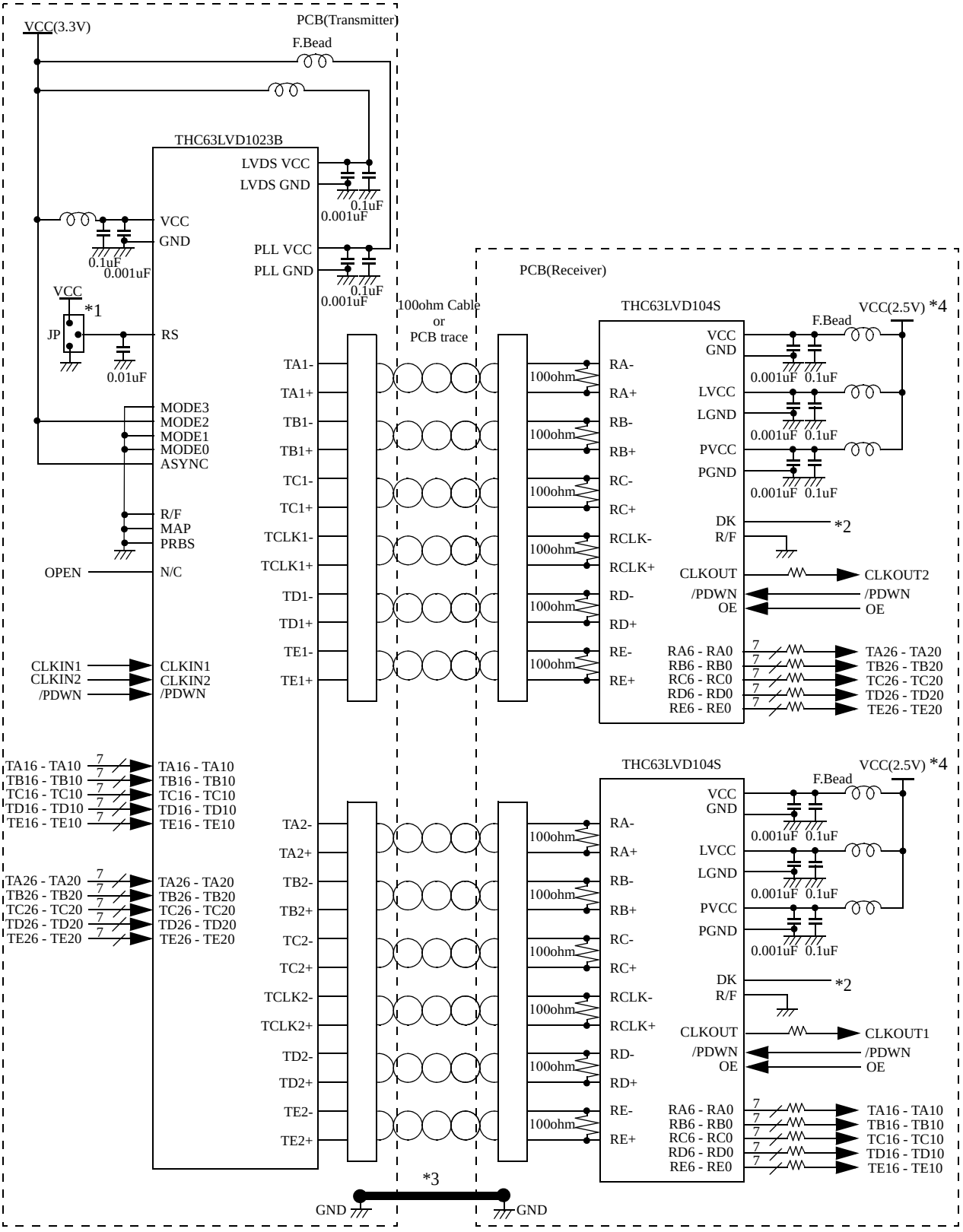
Fig. 4-5

6) Asynchronous Mode (TTL/CMOS Input: 20~112MHz)

Example :

THC63LVD1023B: Falling edge / 10bit / Asynchronous Mode / Crosspoint Switch On

THC63LVD104S : Falling edge / 10bit



*1 : If RS pin tied to VCC, LVDS swing is 350mV.
If RS pin tied to GND, LVDS swing is 200mV.

*2: Refer to datasheet

*3: Connect each PCB GND

*4: Supply voltage of THC63LVD104S is 2.5V(Typ).

Fig. 4-6

5. Note

1)Output Control

THC63LVD1023B

/PDWN	Input(TTL)	Output(LVDS)
L	Open or Hi-z	Hi-z
L	Input CLK	Hi-z
H	Open or Hi-z	Hi-z
H	Input CLK *1	Data, CLK Out

THC63LVD1024 (THC63LVD104S)

/PDWN	OE	Input(LVDS)	Output(TTL)
L	L	Open or Hi-z	Hi-z
L	L	Input CLK	Hi-z
L	H	Open or Hi-z	All Low
L	H	Input CLK	All Low
H	L	Open or Hi-z	Hi-z
H	L	Input CLK	Hi-z
H	H	Open or Hi-z	All Low
H	H	Input CLK *1 *2	Data *2, CLK Out

*1 With in the range of Recommended Operating Conditions. Refer to Recommended Operating Conditions on data sheet. Without the range, the Output(TTL) may unfixed Data, CLK Out.

*2 Open or Hi-z Input Data channel outputs unfixed Data(TTL).

2)Power On Sequence

Power on THC63LVD1023B after THC63LVD1024. If it is not avoidable, please contact to

mspsupport@thine.co.jp (for FAE mailing list)

3)Cable Connection and Disconnection

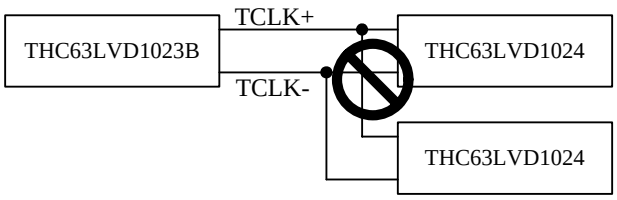
Don't connect and disconnect the LVDS cable , when the power is supplied to the system.

4)GND Connection

Connect the each GND of the PCB which THC63LVD1023B and THC63LVD1024 on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

5)Multi Drop Connection

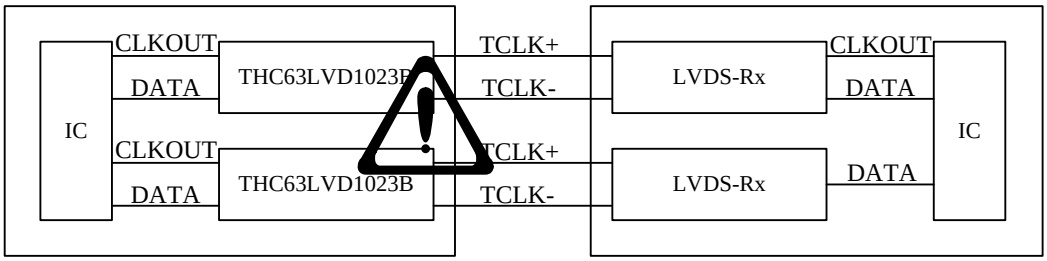
Multi drop connection is not recommended.

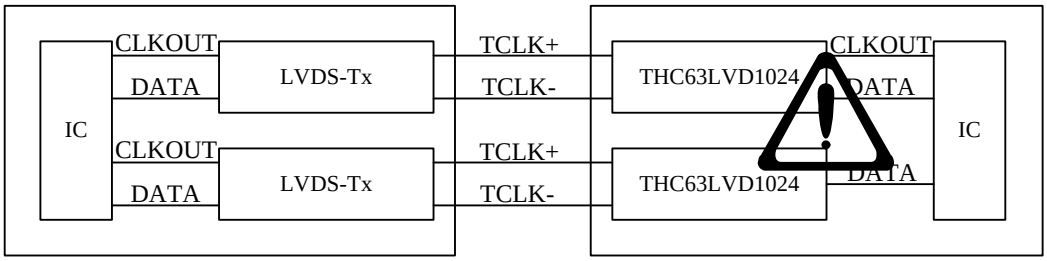


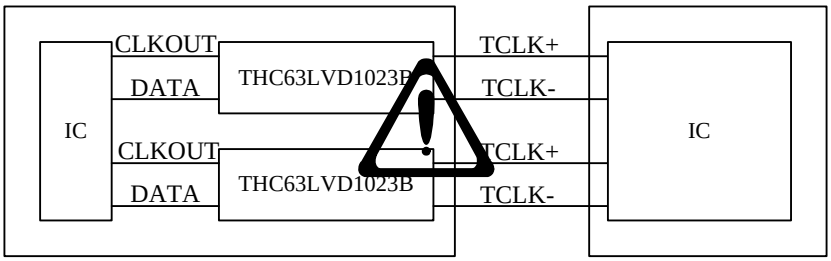
6)Asynchronous use

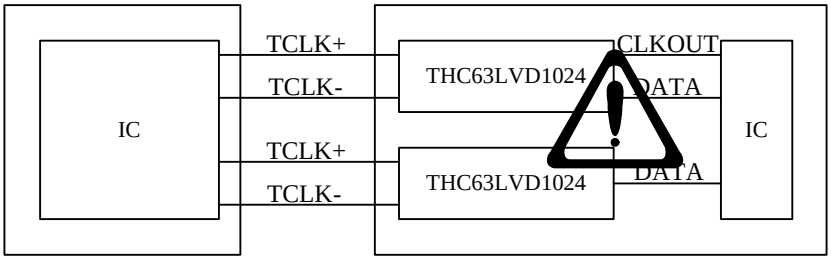
Asynchronous use such as following systems are not recommended. If it is not avoidable, please contact to

mspsupport@thine.co.jp (for FAE mailing list)









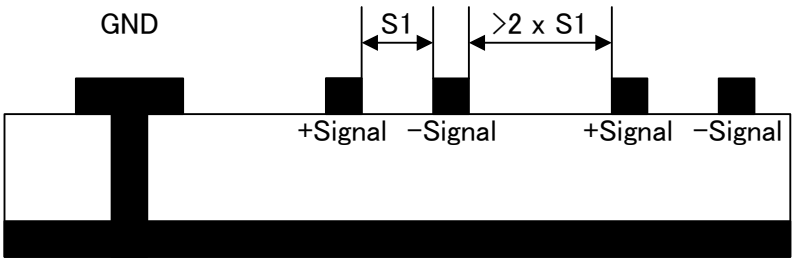
6. PCB Design Guide Line

General Guideline

- Use 4 layer PCB (minimum).
- Locate by-pass capacitors adjacent to the device pins as close as possible.
- Make the loop minimum which is consist of Power line and Gnd line.

LVDS Traces

- Interconnecting media between Transmitter and Receiver (i.e. PCB trace, connector, and cable) should be well balanced.(Keep all these differential impedance and the length of media as same as possible.).
- Minimize the distance between traces of a pair (S1) to maximize common mode rejection. See following figure.
- Place adjacent LVDS trace pair at least twice (>2 x S1) as far away as much as possible.
- Avoid 90 degree bends.
- Minimize the number of VIA on LVDS traces.
- Match impedance of PCB trace, connector, media (cable) and termination to minimize reflections (emissions) for cabled applications (typically 100ohm differential mode characteristic impedance).
- Place Terminal Resister adjacent to the Receiver.



Attentions and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
3. This material contains our copy right, know-how or other proprietary. Copying or disclosing to third parties the contents of this material without our prior permission is prohibited.
4. Note that if infringement of any third party's industrial ownership should occur by using this product, we will be exempted from the responsibility unless it directly relates to the production process or functions of the product.
5. This product is presumed to be used for general electric equipment, not for the applications which require very high reliability (including medical equipment directly concerning people's life, aerospace equipment, or nuclear control equipment). Also, when using this product for the equipment concerned with the control and safety of the transportation means, the traffic signal equipment, or various Types of safety equipment, please do it after applying appropriate measures to the product.
6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

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E-mail:sales@thine.co.jp