Application Note	*THAN0078_Rev.1.1_E*

THC63LVD823(B)/THC63LVD824A Application Note

Mode settings, System Diagram and PCB Design Guide

1.Mode Settings

THC63LVD823(B)

		MODE1	MODE0	DDRN	O/E
Input/Output	Option	Input mode H: Single L: Dual	Output mode H: Single L: Dual	DDR H or Hi-Z: DDR off L: DDR on	Output Enable -
Single In/ Single Out	Output Disable(Hi-Z)	H	H	*	L
	Output Enable(Fig2-1,3-1)	H	H	*	H
Single In/ Dual Out	Output Disable(Hi-Z)	H	L	*	L
	Output Enable/DDR off(Fig2-2,3-4)	H	L	H or Hi-Z	H
	Output Enable/DDR on(Fig2-3,3-4)	H	L	L	H
Dual In/ Single Out	Output Disable(Hi-Z)	L	H	*	L
	Output Enable(Fig2-4,3-2)	L	H	*	H
Dual In/ Dual Out	Output Disable(Hi-Z)	L	L	*	L
	Output Enable(Fig2-5,3-5)	L	L	*	H

THC63LVD824**A**

		MODE1	MODE0
Input/Output	Option	Output mode L: Dual	Input mode H: Single L: Dual
Single In/ Dual Out	Output Enable(Fig2-6,3-1)	L	H
Dual In/ Dual Out	Output Enable(Fig2-7,3-5)	L	L

2.Signal Flow for Each Setting

THC63LVD823(B)

Single In / Single Out

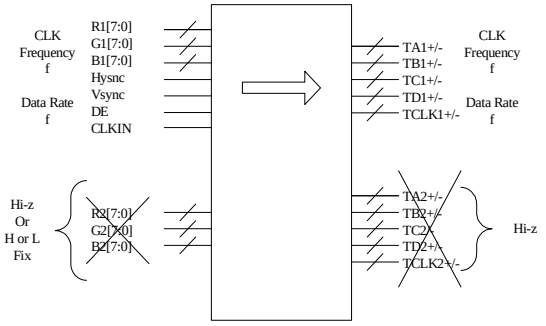


Fig2-1

Single In / Dual Out
DDR off

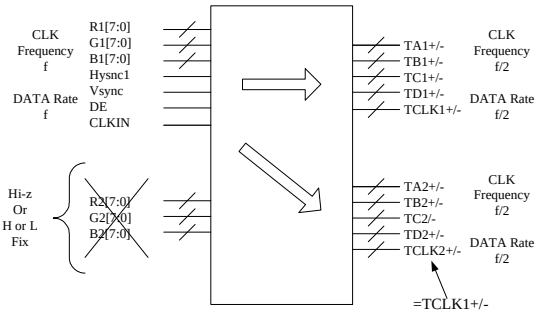


Fig2-2

Single In / Dual Out
DDR on

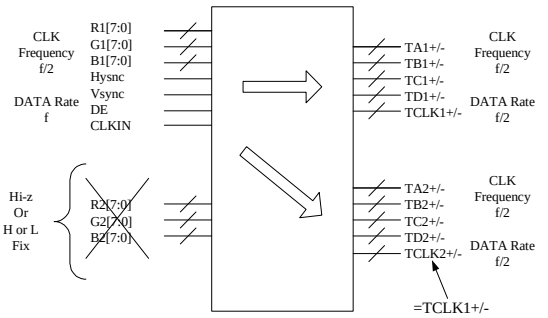


Fig2-3

Dual In / Single Out

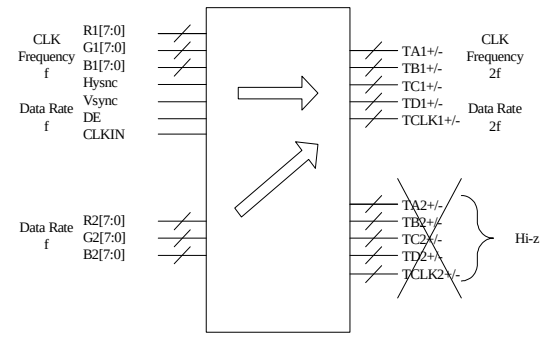


Fig2-4

Dual In / Dual Out

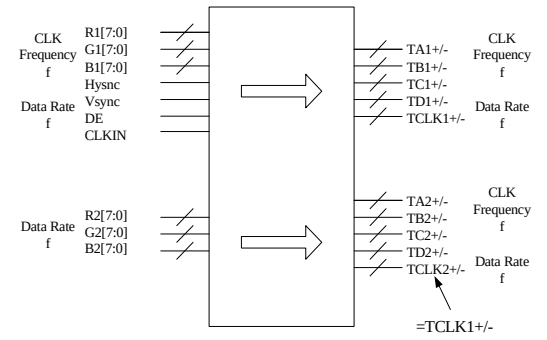


Fig2-5

THC63LVD824A

Single In / Dual Out

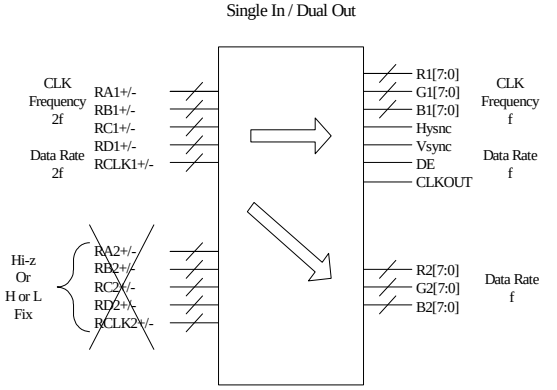


Fig2-6

Dual In / Dual Out

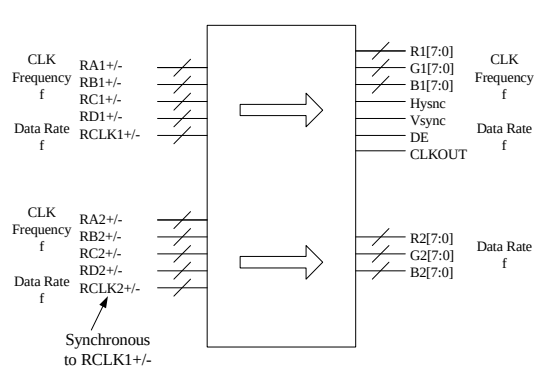
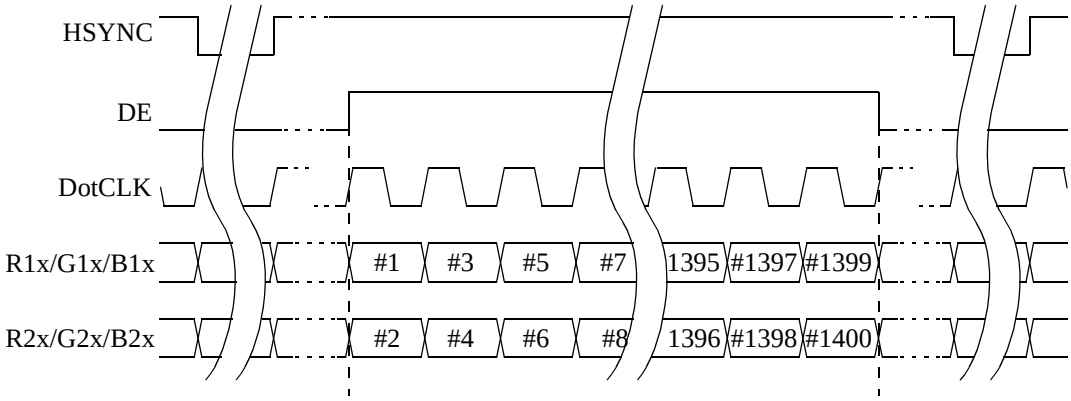
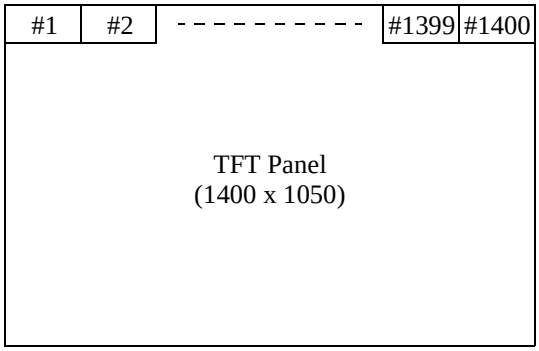


Fig2-7

3.TTL DATA Timing Diagram

Following are THC63LVD823(B) TTL data input timing example for SXGA+(1400 x 1050).





Note:

1)

	R1x	G1x	B1x	R2x	G2x	B2x
MSB	R17	G17	B17	R27	G27	B27
	R16	G16	B16	R26	G26	B26
	R15	G15	B15	R25	G25	B25
	R14	G14	B14	R24	G24	B24
	R13	G13	B13	R23	G23	B23
	R12	G12	B12	R22	G22	B22
	R11	G11	B11	R21	G21	B21
LSB	R10	G10	B10	R20	G20	B20

2) For single and dual link applications, min. pulse width of HSYNC/VSYNC/DE are 2pixels.

1) Single Link(1)

Example :
THC63LVD823(B) : Falling edge / 8bit / Single in(TTL)-Single out(LVDS)
THC63LVD824A : Falling edge / 8bit / Single in(LVDS)-Dual out(TTL) / Output driverbility Low

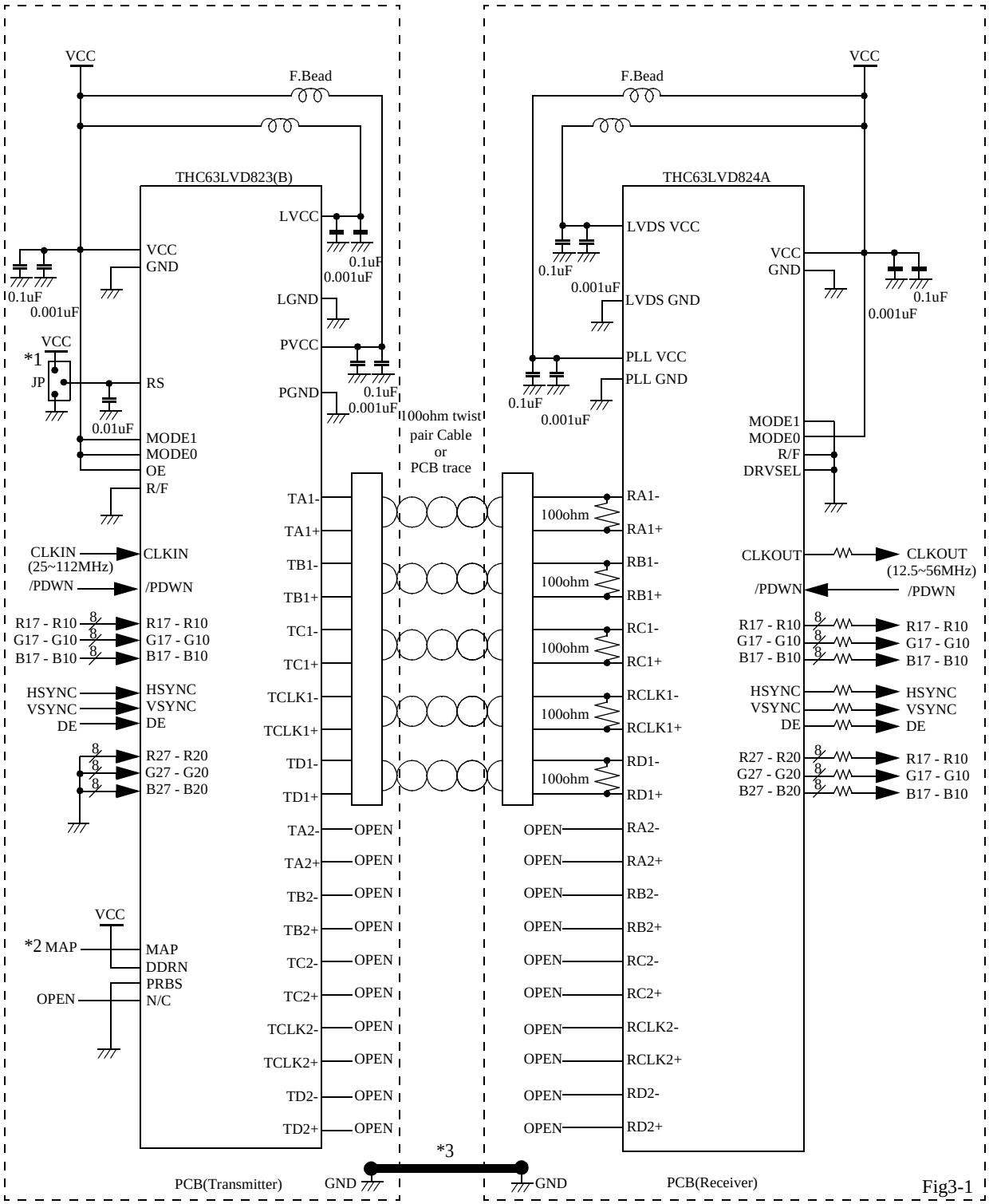


Fig3-1

*1 : If RS pin tied to VCC, LVDS swing is 350mV.
If RS pin tied to GND, LVDS swing is 200mV.
*2: Refer to datasheet
*3: Connect each PCB GND

2) Single Link(2)

Example :

THC63LVD823(B) : Falling edge / 8bit / Dual in(TTL)-Single out(LVDS)

THC63LVD824A : Falling edge / 8bit / Single in(LVDS)-Dual out(TTL) / Output driverbility Low

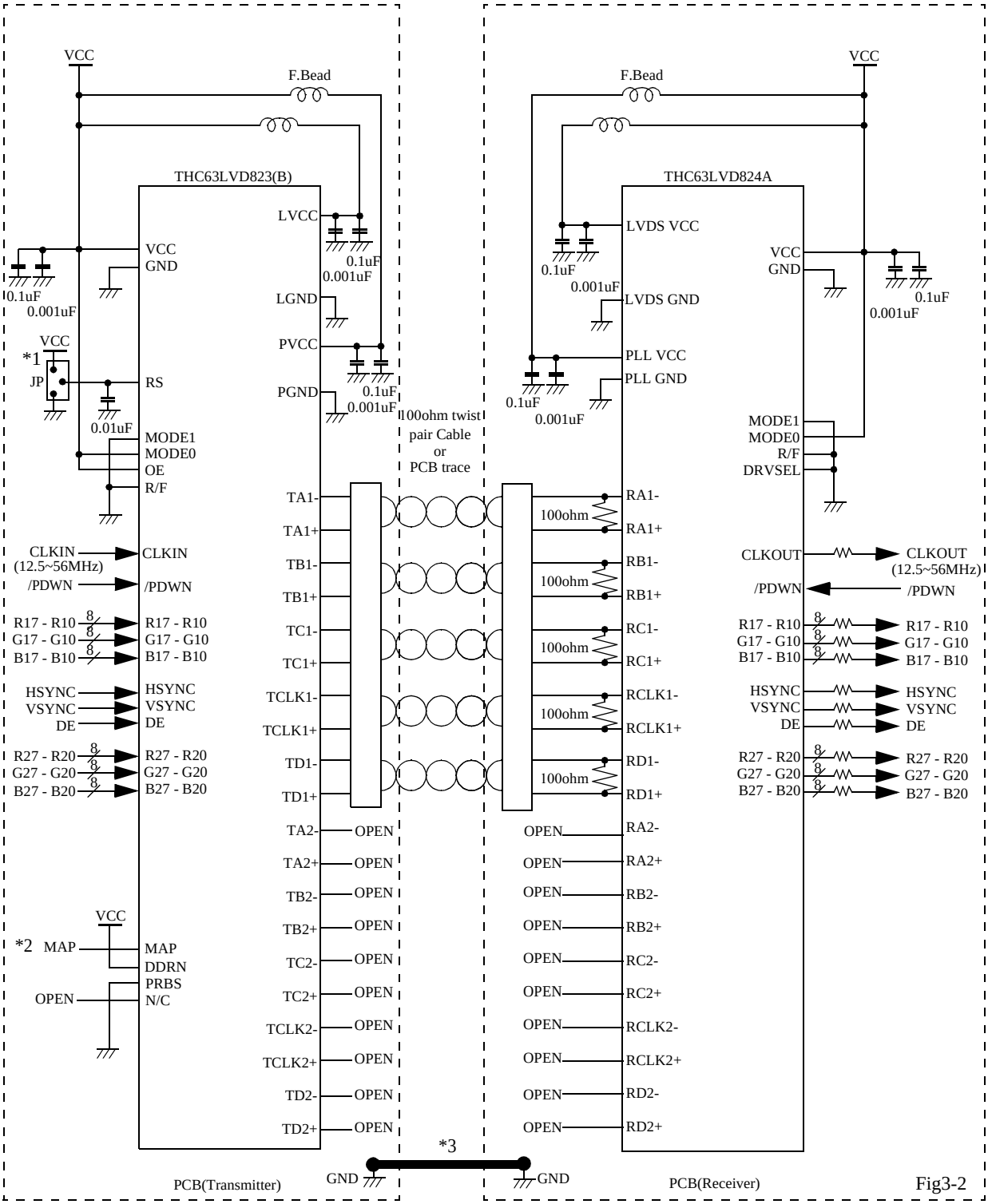


Fig3-2

*1 : If RS pin tied to VCC, LVDS swing is 350mV.
If RS pin tied to GND, LVDS swing is 200mV.

*2: Refer to datasheet

*3: Connect each PCB GND

3) Single Link(3)

Example :

THC63LVD823(B) : Falling edge / 6bit / Dual in(TTL)-Single out(LVDS)

THC63LVD824A : Falling edge / 6bit / Single in(LVDS)-Dual out(TTL) / Output driverbility Low

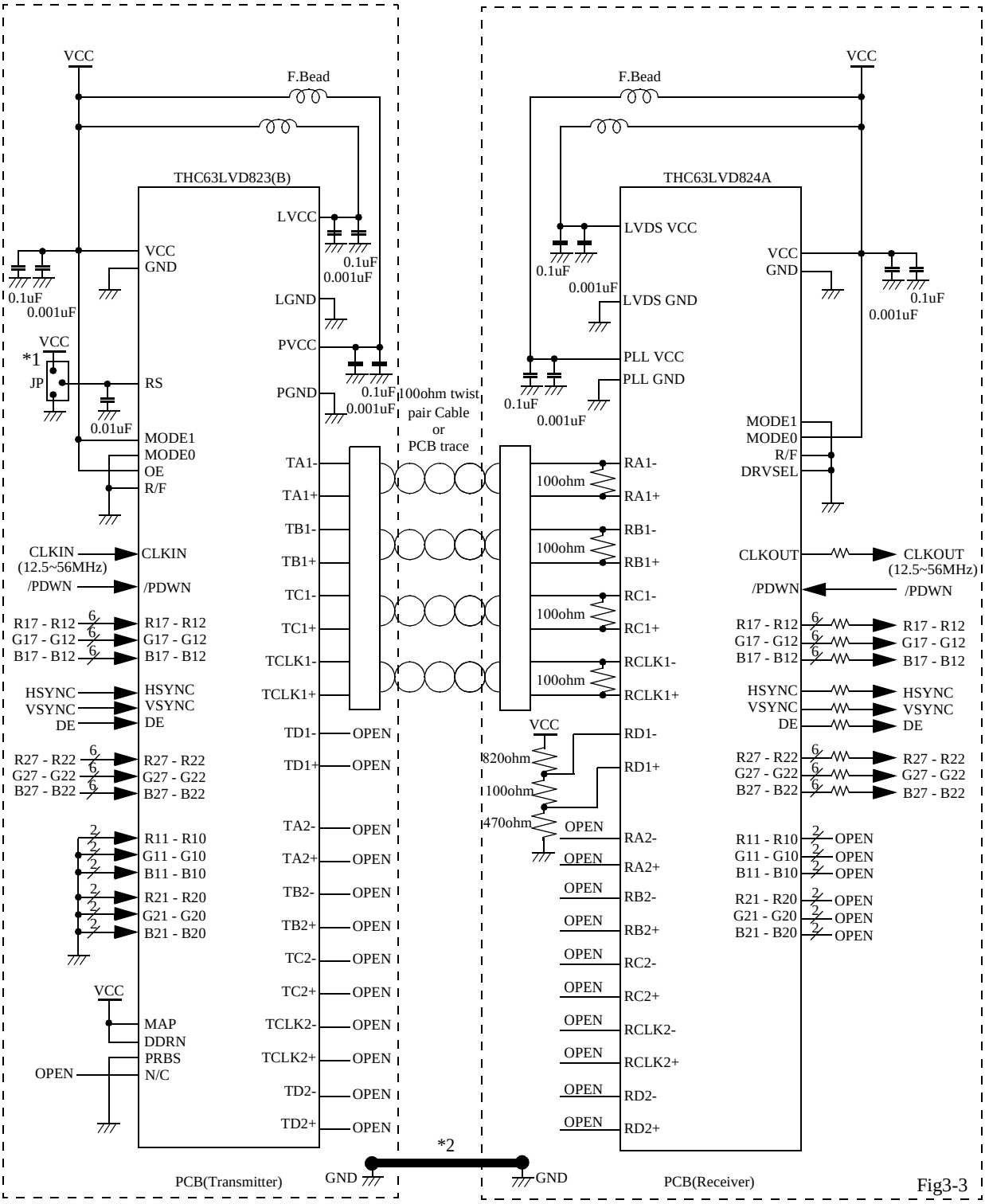


Fig3-3

*1 : If RS pin tied to VCC, LVDS swing is 350mV.
If RS pin tied to GND, LVDS swing is 200mV.

*2: Connect each PCB GND

4) Dual Link(1)

Example :
THC63LVD823(B) : Falling edge/ 8bit / Single in(TTL)-Dual out(LVDS) / DDR Off or On
THC63LVD824A : Falling edge / 8bit / Dual in(LVDS)-Dual out(TTL) / Output driverbility Low

Note1: tDEINT = tTCIP*2n (n=integer)
Note2: tDEINT >= 4*tTCIP
Note3: tDEH >= 2k*tTCIP, tDEL >= 2m*tTCIP (k,m = integer)
(tDEINT = DE Period, tTCIP = CLKIN Period, tDEH = DE High Time, tDEL = DE Low Time) *2

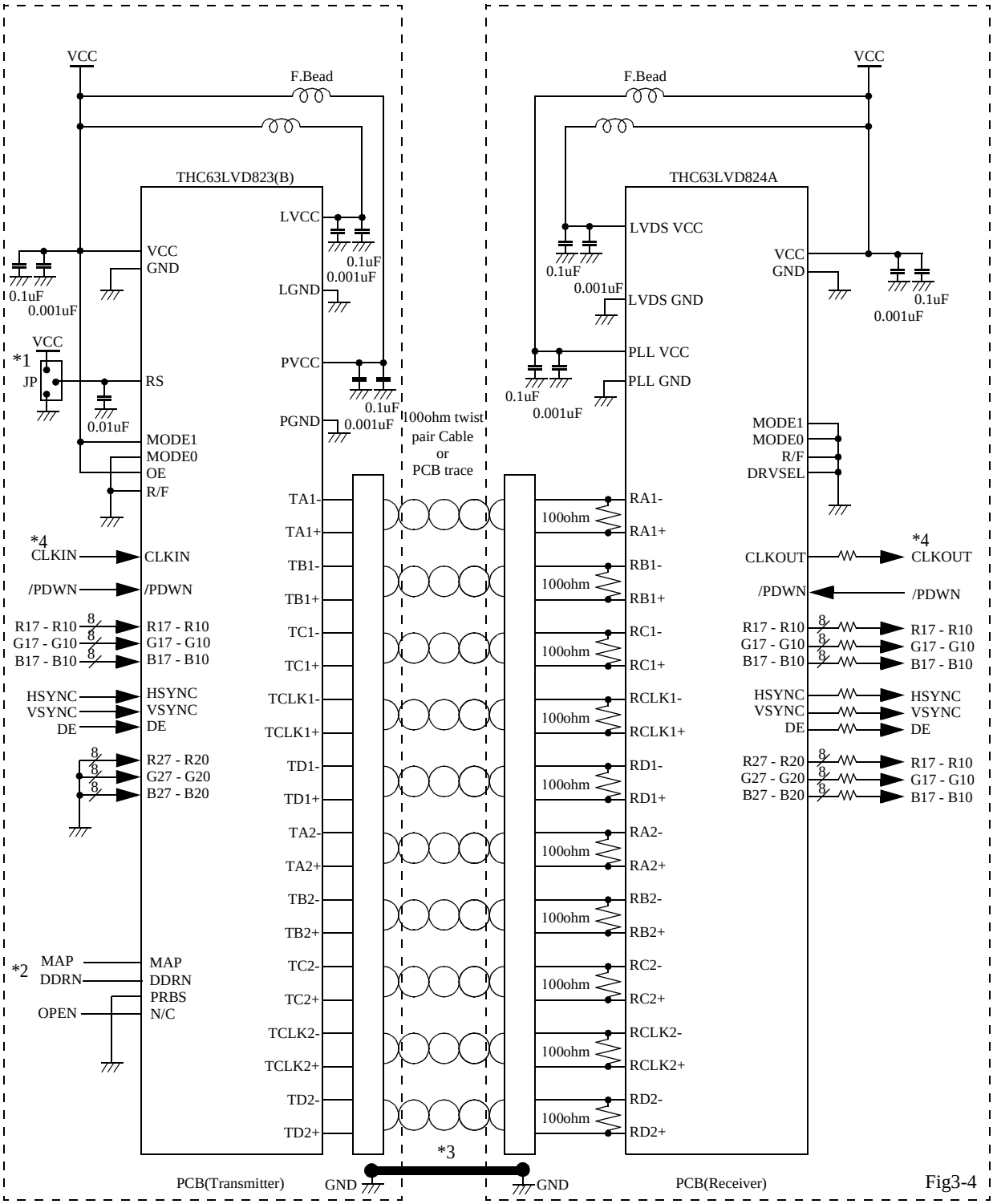


Fig3-4

*1 : If RS pin tied to VCC, LVDS swing is 350mV.
If RS pin tied to GND, LVDS swing is 200mV.
*2: Refer to datasheet

*3: Connect each PCB GND

*4

DDR	CLKIN	CLKOUT
off	50~150MHz	25~75MHz
on	25~75MHz	12.5~37.5MHz

5) Dual Link(2)

Example :
THC63LVD823(B): Falling edge / 8bit / Dual in(TTL)-Dual out(LVDS)
THC63LVD824A : Falling edge / 8bit / Dual in(LVDS)-Dual out(TTL) / Output driverbility Low

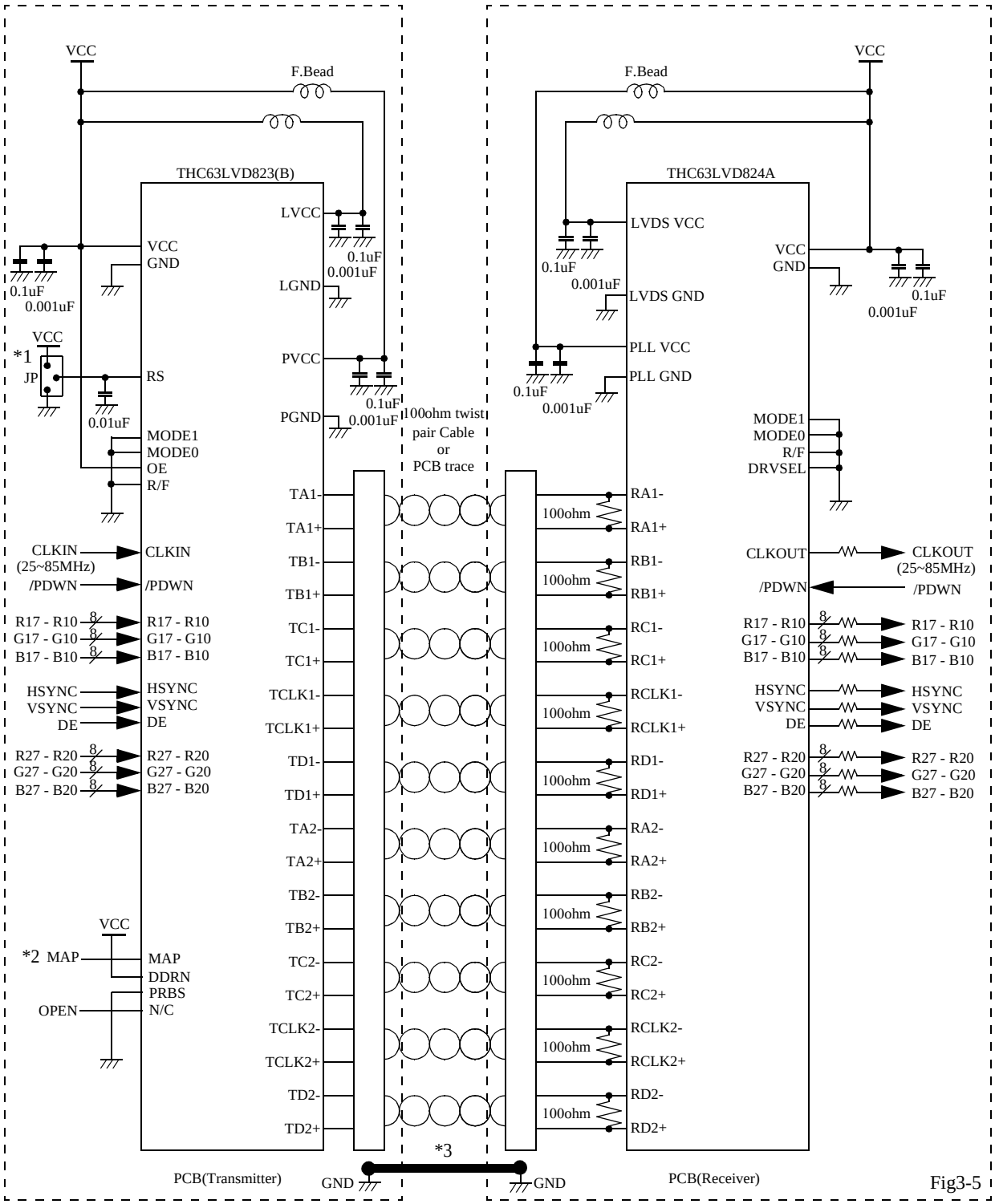


Fig3-5

*1 : If RS pin tied to VCC, LVDS swing is 350mV.
If RS pin tied to GND, LVDS swing is 200mV.
*2: Refer to datasheet
*3: Connect each PCB GND

4. Note

1)Output Control

THC63LVD823(B)

/PDWN	OE	Input(TTL)	Output(LVDS)
L	L	Open or Hi-z	Hi-z
L	L	Input CLK	Hi-z
L	H	Open or Hi-z	Hi-z
L	H	Input CLK	Hi-z
H	L	Open or Hi-z	Hi-z
H	L	Input CLK	Hi-z
H	H	Open or Hi-z	Hi-z
H	H	Input CLK *1	Data, CLK Out

THC63LVD824A

/PDWN	Input(LVDS)	Output(TTL)
L	Open or Hi-z	All Low
L	Input CLK	All Low
H	Open or Hi-z	Unstable
H	Input CLK *1 *2	Data *2, CLK Out

*1 With in the range of Recommended Operating Conditions. Refer to Recommended Operating Conditions on data sheet. Without the range, the Output(TTL) may unfixed Data, CLK Out.

*2 Open or Hi-z Input Data channel outputs unfixed Data(TTL).

2)Power On Sequence

Power on THC63LVD823(B) after THC63LVD824A.

3)Cable Connection and Disconnection

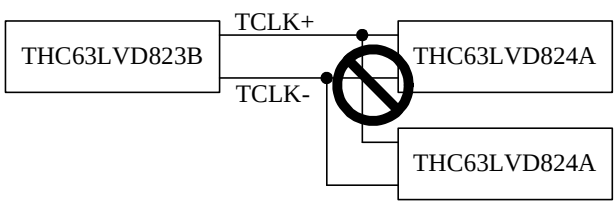
Don't connect and disconnect the LVDS cable , when the power is supplied to the system.

4)GND Connection

Connect the each GND of the PCB which THC63LVD823(B) and THC63LVD824A on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

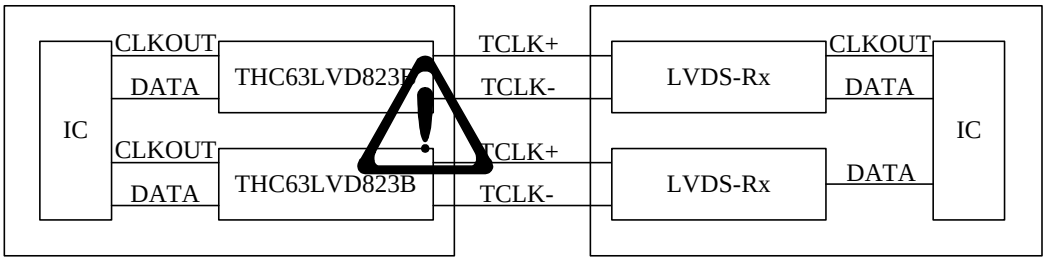
5)Multi Drop Connection

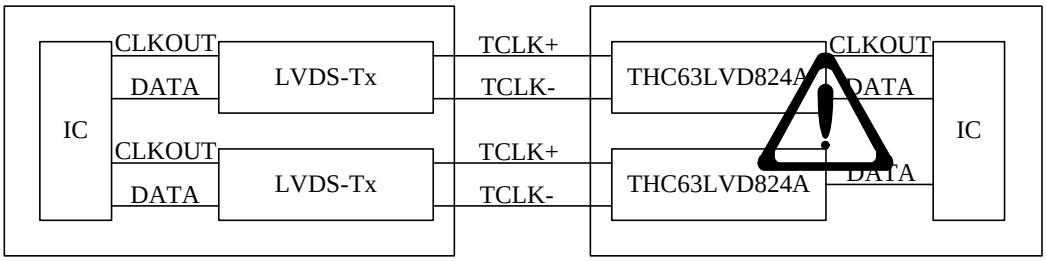
Multi drop connection is not recommended.

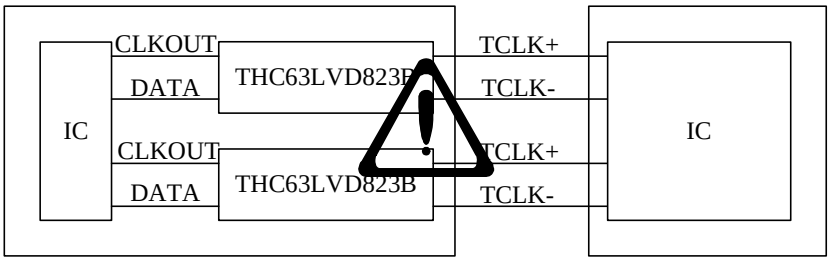


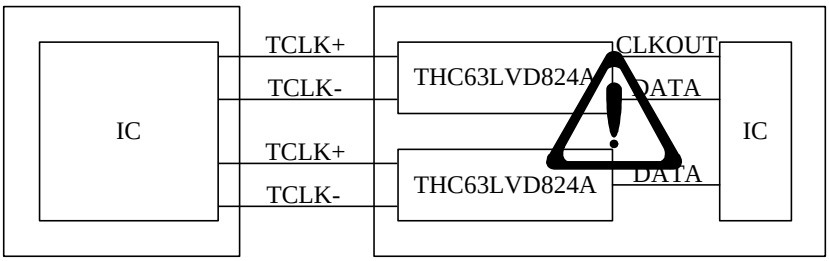
6)Asynchronous use

Asynchronous use such as following systems are not recommended.









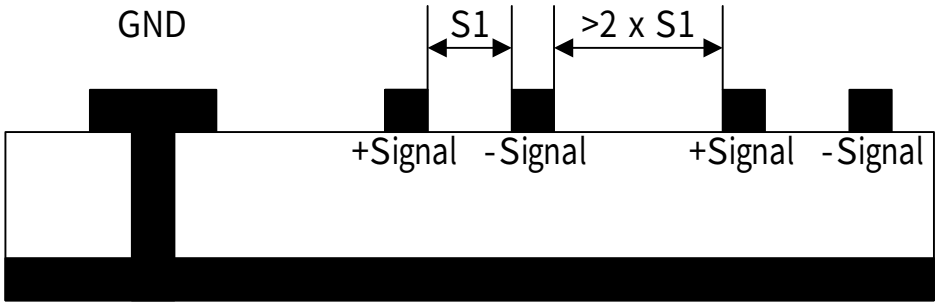
5. PCB Design Guide Line

General Guideline

- Use 4 layer PCB (minimum).
- Locate by-pass capacitors adjacent to the device pins as close as possible.
- Make the loop minimum which is consist of Power line and Gnd line.

LVDS Traces

- Interconnecting media between Transmitter and Receiver (i.e. PCB trace, connector, and cable) should be well balanced.(Keep all these differential impedance and the length of media as same as possible.).
- Minimize the distance between traces of a pair (S1) to maximize common mode rejection. See following figure.
- Place adjacent LVDS trace pair at least twice (>2 x S1) as far away as much as possible.
- Avoid 90 degree bends.
- Minimize the number of VIA on LVDS traces.
- Match impedance of PCB trace, connector, media (cable) and termination to minimize reflections (emissions) for cabled applications (typically 100ohm differential mode characteristic impedance).
- Place Terminal Resister adjacent to the Receiver.



Attentions and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
3. This material contains our copy right, know-how or other proprietary. Copying or disclosing to third parties the contents of this material without our prior permission is prohibited.
4. Note that if infringement of any third party's industrial ownership should occur by using this product, we will be exempted from the responsibility unless it directly relates to the production process or functions of the product.
5. This product is presumed to be used for general electric equipment, not for the applications which require very high reliability (including medical equipment directly concerning people's life, aerospace equipment, or nuclear control equipment). Also, when using this product for the equipment concerned with the control and safety of the transportation means, the traffic signal equipment, or various Types of safety equipment, please do it after applying appropriate measures to the product.
6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

THine Electronics, Inc.
E-mail:sales@thine.co.jp