Application Note	*THAN0147_Rev.1.00_E*

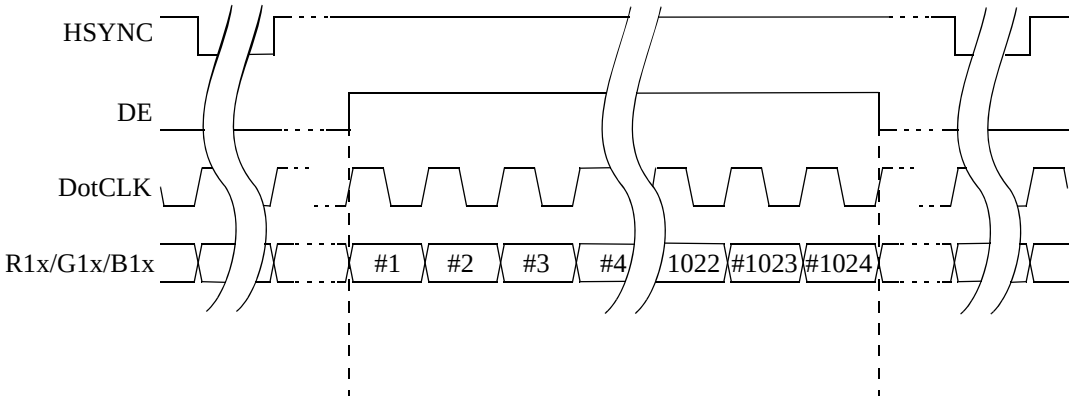
THC63LVDM83C(5S)/THC63LVDF84B(5S)
Application Note
System Diagram and PCB Design Guide Line

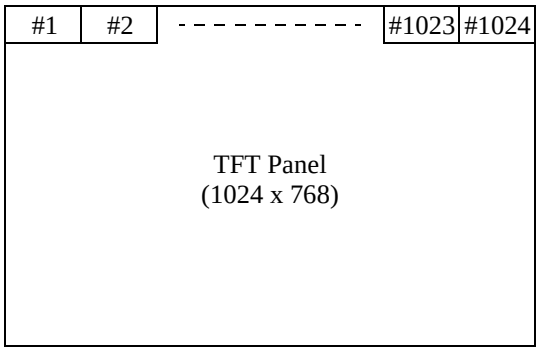
Date	Revision
2013.5.7	THAN0147_Rev.1.00_E

Contents

1. TTL DATA Timing Diagram

Following are THC63LVDM83C(5S) TTL data input timing example for XGA(1024 x 768).

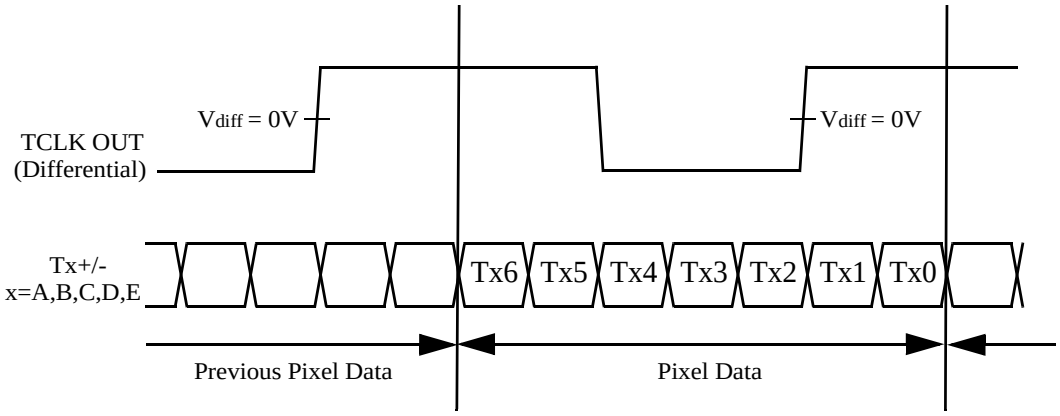




Note:

	Red	Green	Blue
MSB	R7	G7	B7
	R6	G6	B6
	R5	G5	B5
	R4	G4	B4
	R3	G3	B3
6bit LSB	R2	G2	B2
	R1	G1	B1
8bit LSB	R0	G0	B0

2.LVDS DATA Timing Diagram



THC63LVDM83C(5S)/THC63LVDF84B(5S) Pixel Data Assign (6bit,8bit Application)

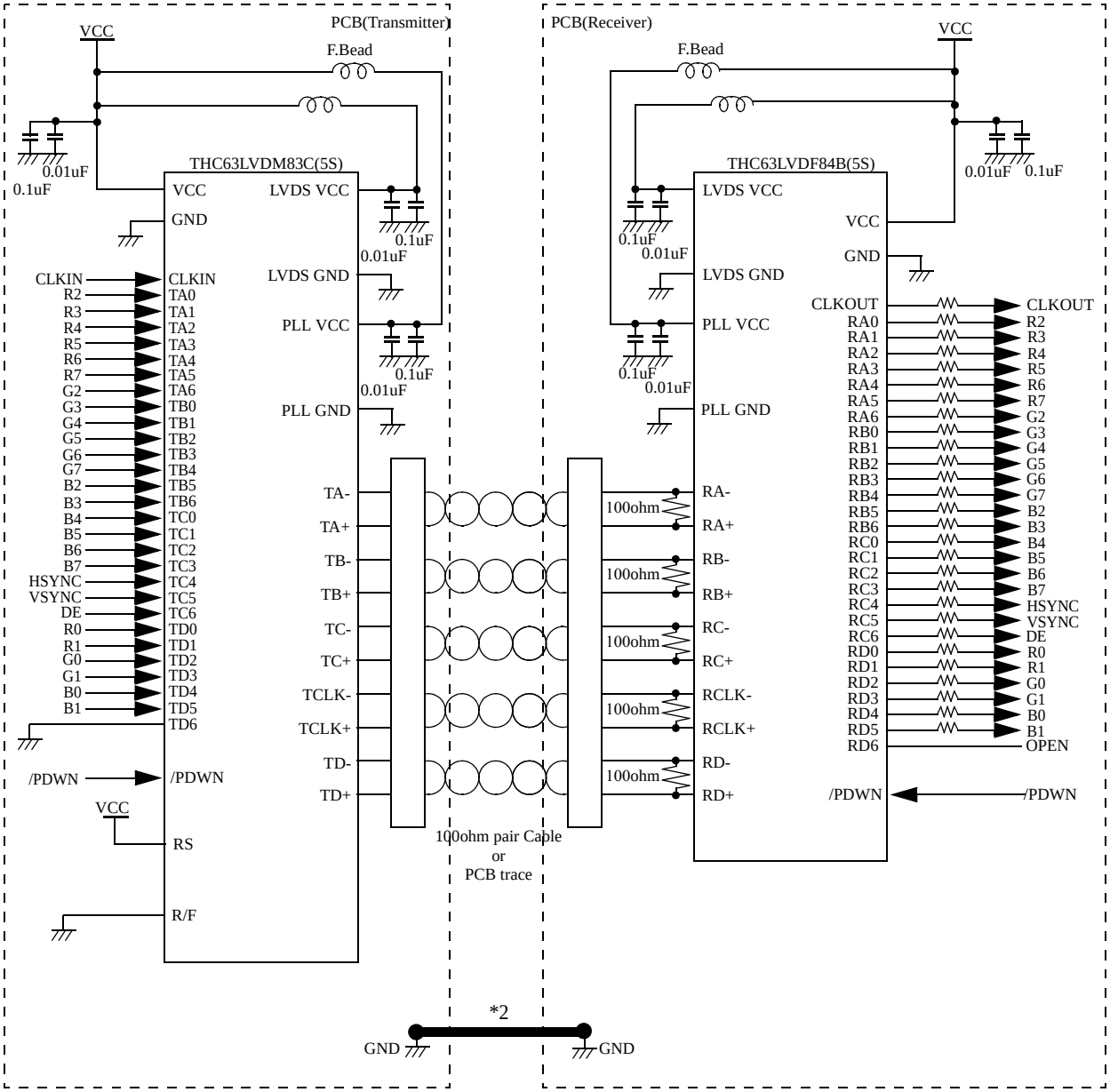
	6bit	8bit
TA0	R2	R2
TA1	R3	R3
TA2	R4	R4
TA3	R5	R5
TA4	R6	R6
TA5	R7	R7
TA6	G2	G2
TB0	G3	G3
TB1	G4	G4
TB2	G5	G5
TB3	G6	G6
TB4	G7	G7
TB5	B2	B2
TB6	B3	B3
TC0	B4	B4
TC1	B5	B5
TC2	B6	B6
TC3	B7	B7
TC4	Hsync	Hsync
TC5	Vsync	Vsync
TC6	DE	DE
TD0	-	R0
TD1	-	R1
TD2	-	G0
TD3	-	G1
TD4	-	B0
TD5	-	B1
TD6	-	N/A

Note:For 6bit application,use A~C channel and open TD+/- pin.

3. Example of System Diagram

1)8 bit TTL/CMOS Input(20~85MHz)

Example:
THC63LVDM83C(5S) :Falling edge/Normal swing
THC63LVDF84B(5S) :Falling edge

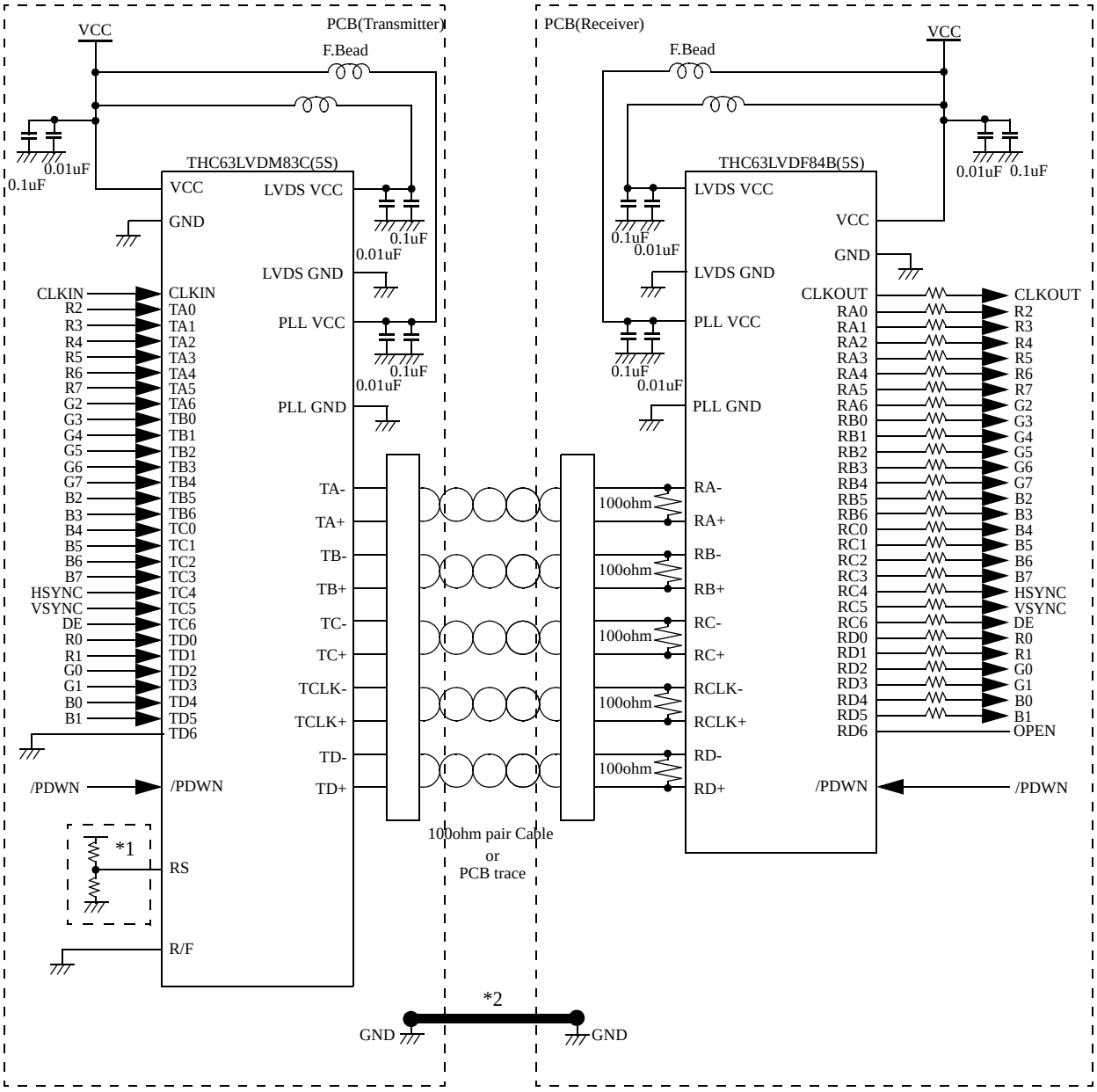


*1:If RS pin is tied to VCC, LVDS swing is 350mV.
If RS pin is tied to GND, LVDS swing is 200mV.

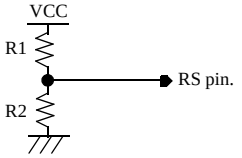
*2:Connect each PCB GND

2)8 bit Small Swing Input(20~85MHz)

Example:
THC63LVDM83C(5S) :Small Swing input/Falling edge
THC63LVDF84B(5S) :Falling edge



*1:RS pin acts as VREF input pin when input voltage is set to half of high level signal input.

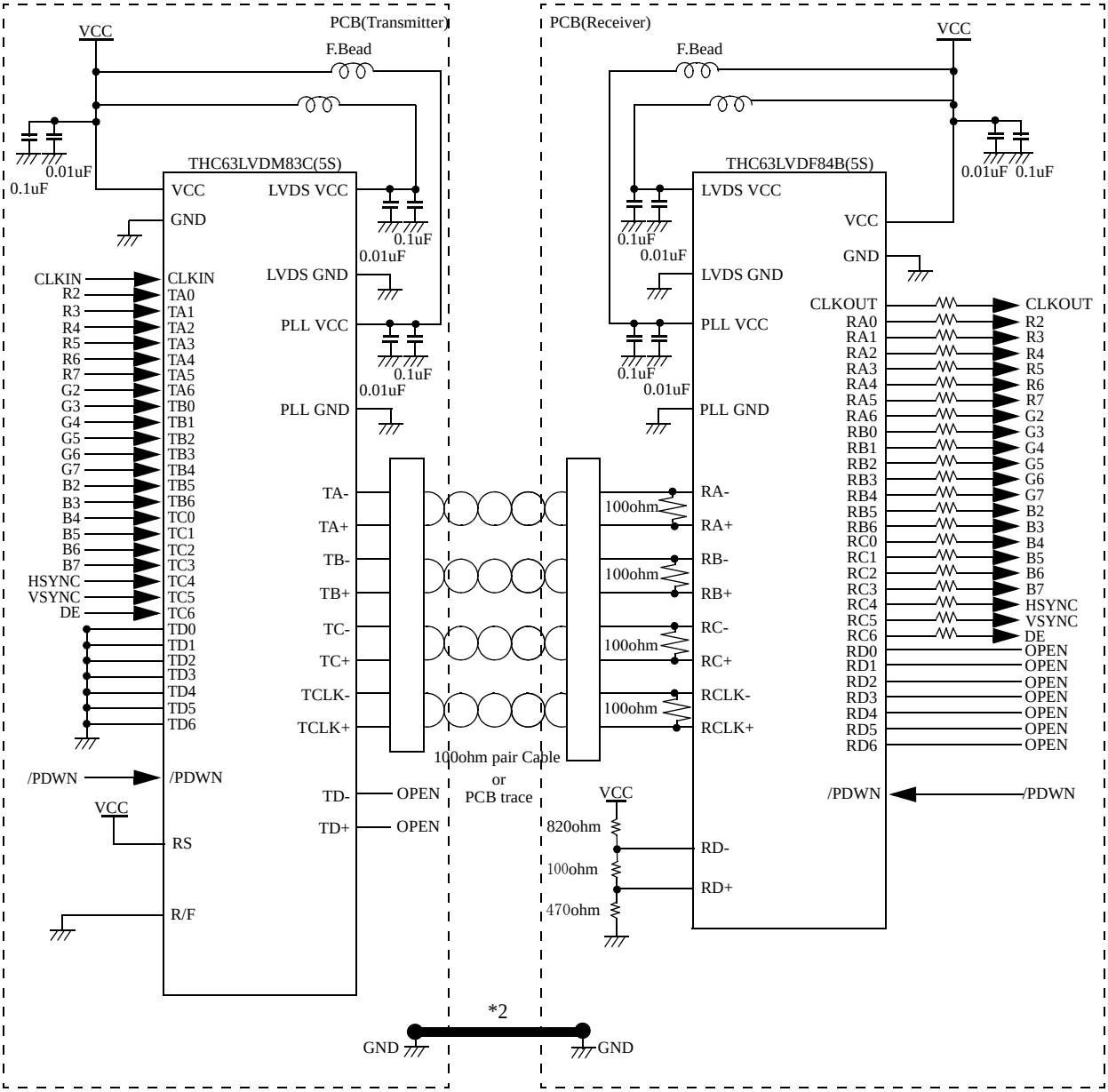


Example for Small Swing input (R1,R2)=(3.3kohm,1kohm~2.2kohm)

*2:Connect each PCB GND

3)6bit TTL/CMOS Input(20~85MHz)

Example:
THC63LVDM83C(5S) :Falling edge/Normal swing
THC63LVDF84B(5S) :Falling edge



*1:If RS pin is tied to VCC, LVDS swing is 350mV.
If RS pin is tied to GND, LVDS swing is 200mV.

*2:Connect each PCB GND

4. Note

1)Power On Sequence

Power on THC63LVDM83C(5S) after THC63LVDF84B(5S). If it is not avoidable, please contact to

mspsupport@thine.co.jp (for FAE mailing list)

2)Cable Connection and Disconnection

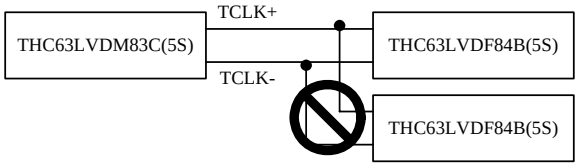
Don't connect and disconnect the LVDS cable , when the power is supplied to the system.

3)GND Connection

Connect the each GND of the PCB which THC63LVDM83C(5S) and THC63LVDF84B(5S) on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

4)Multi Drop Connection

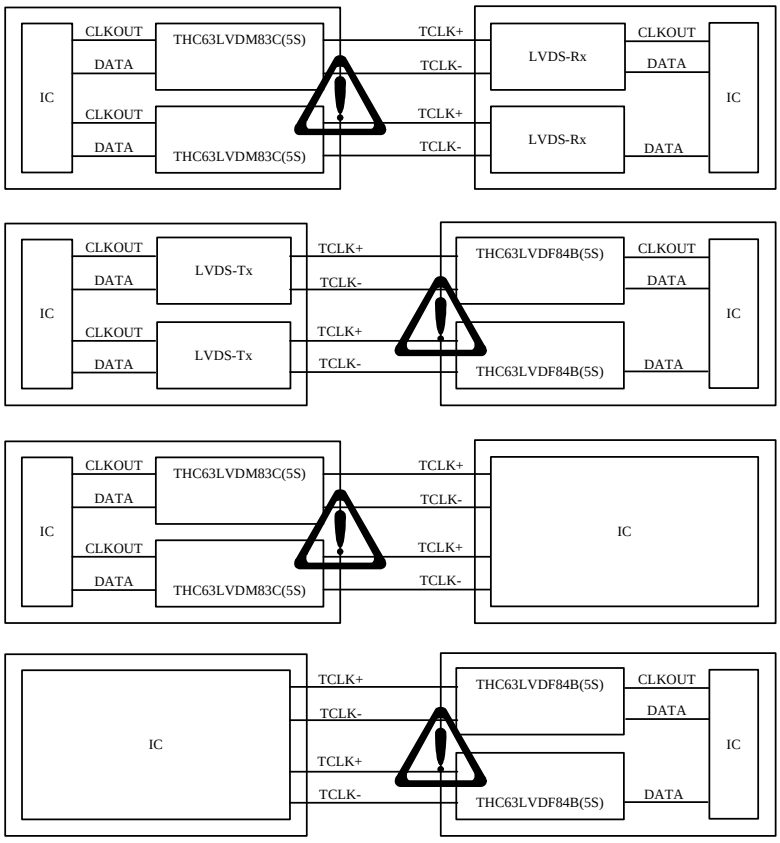
Multi drop connection is not recommended.



5)Asynchronous use

Asynchronous use such as following systems are not recommended. If it is not avoidable, please contact to

mspsupport@thine.co.jp (for FAE mailing list)



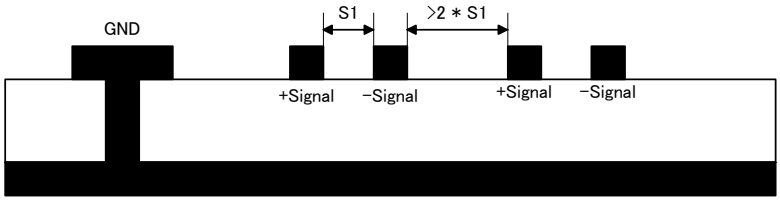
6. PCB Design Guide Line

General Guideline

- Use 4 layer PCB (minimum).
- Locate by-pass capacitors adjacent to the device pins as close as possible.
- Make the loop minimum which is consist of Power line and Gnd line.

LVDS Traces

- Interconnecting media between Transmitter and Receiver (i.e. PCB trace, connector, and cable) should be well balanced.(Keep all these differential impedance and the length of media as same as possible.).
- Minimize the distance between traces of a pair (S1) to maximize common mode rejection. See following figure.
- Place adjacent LVDS trace pair at least twice (>2 x S1) as far away as much as possible.
- Avoid 90 degree bends.
- Minimize the number of VIA on LVDS traces.
- Match impedance of PCB trace, connector, media (cable) and termination to minimize reflections (emissions) for cabled applications (typically 100ohm differential mode characteristic impedance).
- Place Terminal Resister adjacent to the Receiver.



Attentions and Requests

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2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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