Application Note	*THAN0127_Rev.1.40_E*

THCV219/THCV220 Application Note

System Diagram and PCB Design Guideline

Contents

Application Diagrams

RGB24bit per pixel falling edge system with only LOCKN connection

[V-by-One® HS]

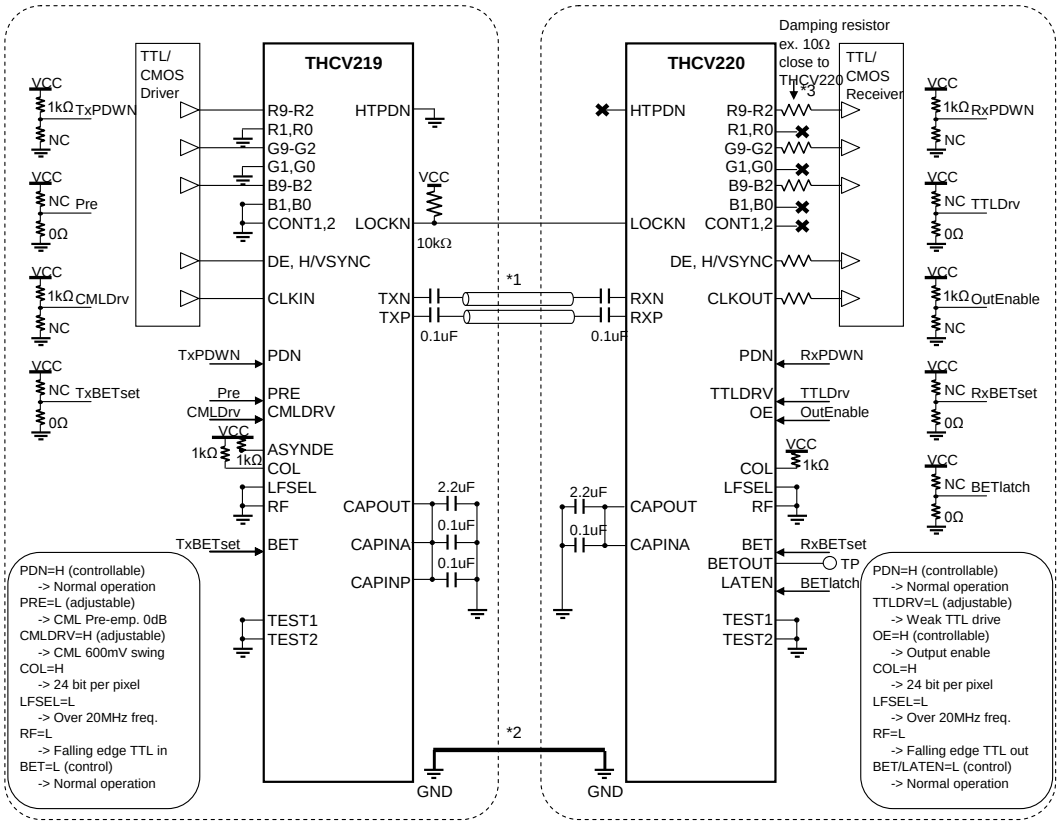
HTPDN connection can be eliminated. Set THCV219 HTPDN **Low** and leave THCV220 HTPDN **Open**.

[THCV219]

PDN can be controlled by external resistor or other driving source like MCU.
Design PRE pin and CMLDRV pin in order to adjust setting appropriate to actual PCB/cable transmission line.
Set COL pin **High** (24bit), LFSEL pin **Low** (over 20MHz) and RF pin **Low** (Falling edge TTL/CMOS input).
BET pin can be used as Bit Error Test entry in actual configuration in order for debug or test purpose.
Unused TTL/CMOS input pins should be connected to **Low** (GND).

[THCV220]

PDN and OE can be controlled by external resistor or other driving source like MCU.
Design TTLDRV pin in order to adjust setting appropriate to actual PCB transmission trace.
Set COL pin **High** (24bit), LFSEL pin **Low** (over 20MHz) and RF pin **Low** (Falling edge TTL/CMOS output).
BET, BETOUT and LATEN pin can be used for Bit Error Test in actual configuration in order for debug or test.
Unused TTL/CMOS output pins should be left **Open**.
Place 10Ω resistor close to outputs, which can be eliminated when freq. is low, trace is short, and TTLDRV=**L**.



*1 indicates microstrip lines or cables with their differential characteristic impedance being 100Ω
*2 Connect GNDs of both Tx and Rx PCB
*3 TTL output dampling resistor can be totally eliminated if freq. is low, trace is short and TTLDRV=L

32bit (RGB30bit and arbitrary 2bit (ex. kHz)) per pixel falling edge with only one pair

[V-by-One® HS]

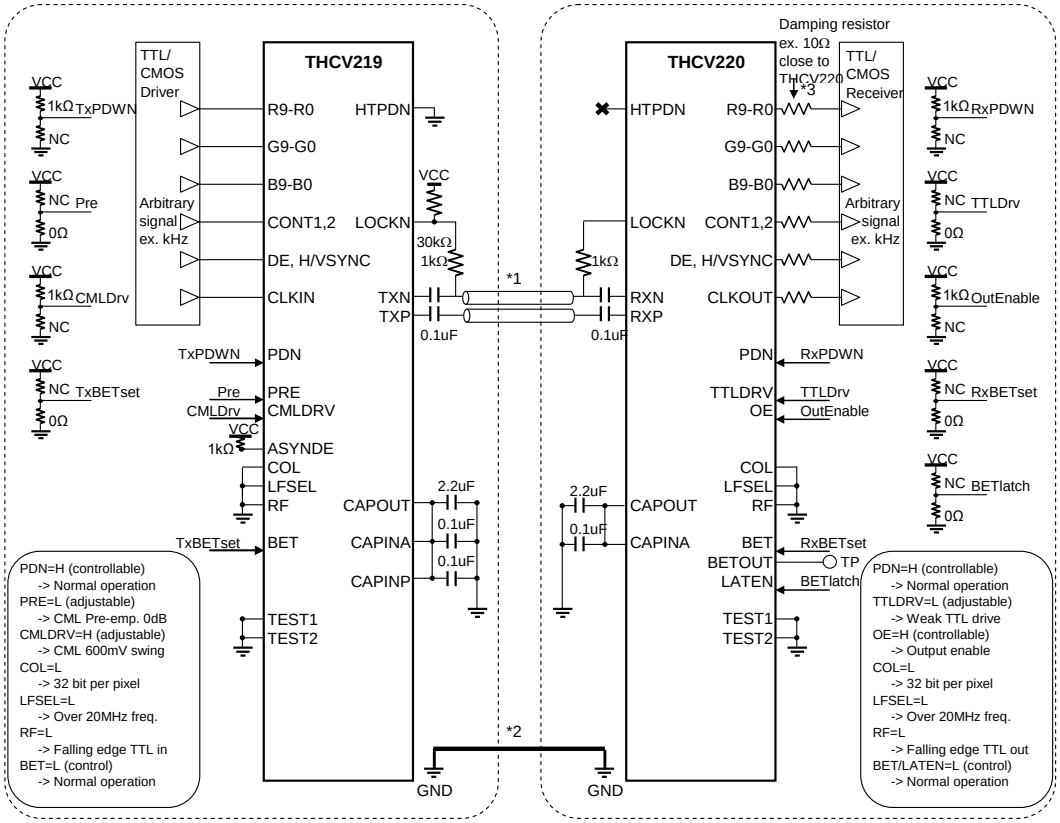
HTPDN connection can be eliminated. Set THCV219 HTPDN **Low** and leave THCV220 HTPDN **Open**.
LOCKN connection can be shared with V-by-One® HS trace. Put 1kΩ resistors on both side.

[THCV219]

PDN can be controlled by external resistor or other driving source like MCU.
Design PRE pin and CMLDRV pin in order to adjust setting appropriate to actual PCB/cable transmission line.
Set COL pin **Low** (32bit), LFSEL pin **Low** (over 20MHz) and RF pin **Low** (Falling edge TTL/CMOS input).
BET pin can be used as Bit Error Test entry in actual configuration in order for debug or test purpose.
Arbitrary slow pulse should be assigned to CTL bits (ex. CONT1,2) for continuous transfer independent of DE

[THCV220]

PDN and OE can be controlled by external resistor or other driving source like MCU.
Design TTLDRV pin in order to adjust setting appropriate to actual PCB transmission trace.
Set COL pin **Low** (32bit), LFSEL pin **Low** (over 20MHz) and RF pin **Low** (Falling edge TTL/CMOS output).
BET, BETOUT and LATEN pin can be used for Bit Error Test in actual configuration in order for debug or test.
Place 10Ω resistor close to outputs, which can be eliminated when freq. is low, trace is short, and TTLDRV=**L**.



*1 indicates microstrip lines or cables with their differential characteristic impedance being 100Ω
*2 Connect GNDs of both Tx and Rx PCB
*3 TTL output dampling resistor can be totally eliminated if freq. is low and trace is short and TTLDRV=L

CCIR601/656 8bit, HS, VS camera image per pixel with only one pair, meters distance

[V-by-One® HS]

HTPDN connection can be eliminated. Set THCV219 HTPDN **Low** and leave THCV220 HTPDN **Open**.

LOCKN connection can be shared with V-by-One® HS trace. Put 1kΩ resistors on both side.

[THCV219]

PDN can be controlled by external resistor or other driving source like MCU.

Set PRE pin and CMLDRV pin **High** for long distance operation.

Set COL pin **High** (24bit), LFSEL pin **Low** (over 20MHz) and RF pin properly (Falling or Rising edge).

BET pin can be used as Bit Error Test entry in actual configuration in order for debug or test purpose.

Camera HSYNC should be connected to THCV219 DE and polarity must be cared by ASYNDE setting.

[THCV220]

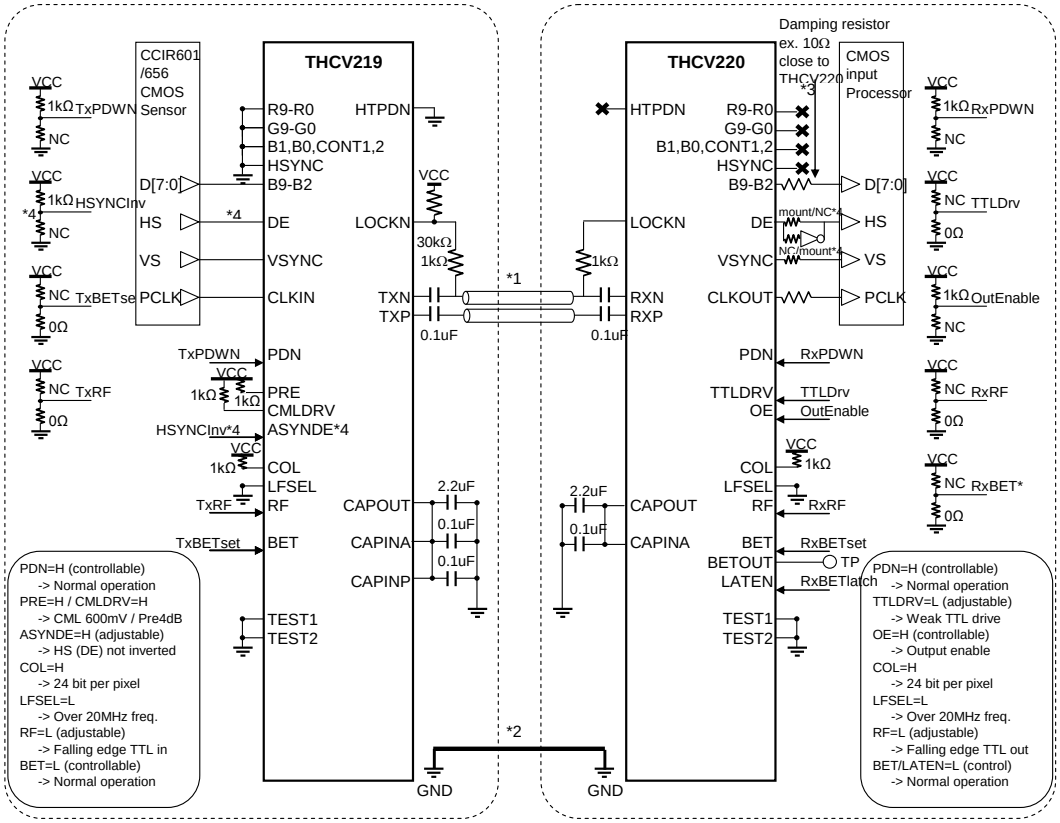
PDN and OE can be controlled by external resistor or other driving source like MCU.

Set COL pin **High** (24bit), LFSEL pin **Low** (over 20MHz) and RF pin properly (Falling or Rising edge).

BET, BETOUT and LATEN pin can be used for Bit Error Test in actual configuration in order for debug or test.

Place 10Ω resistor close to outputs, which can be eliminated when freq. is low, trace is short, and TTLDRV=**L**.

Processor HSYNC should be connected to THCV220 DE and polarity must be cared by external inverter.



*1 indicates microstrip lines or cables with their differential characteristic impedance being 100Ω

*2 Connect GNDs of both Tx and Rx PCB

*3 TTL output dampling resistor can be totally eliminated if freq. is low and trace is short and TTLDRV=L

*4 System HSYNC signal should be matched to Vx1HS DE requirement. Active image should be during DE=H.

CCIR601/656 10bit, HS, VS camera image per pixel with only one pair, meters distance

10 bit least significant two bits are allocated to R19-R18 (default) and B11-B10 (CTL packet in 10 bit mode).
8 bit mode is recommended for long distance transmission; however, sometimes CTL in 10 bit mode are needed.
[V-by-One® HS]
HTPDN connection can be eliminated. Set THCV219 HTPDN **Low** and leave THCV220 HTPDN **Open**.
LOCKN connection can be shared with V-by-One® HS trace. Put 1kΩ resistors on both side.
[THCV219]
PDN can be controlled by external resistor or other driving source like MCU.
Set PRE pin and CMLDRV pin **High** for long distance operation.
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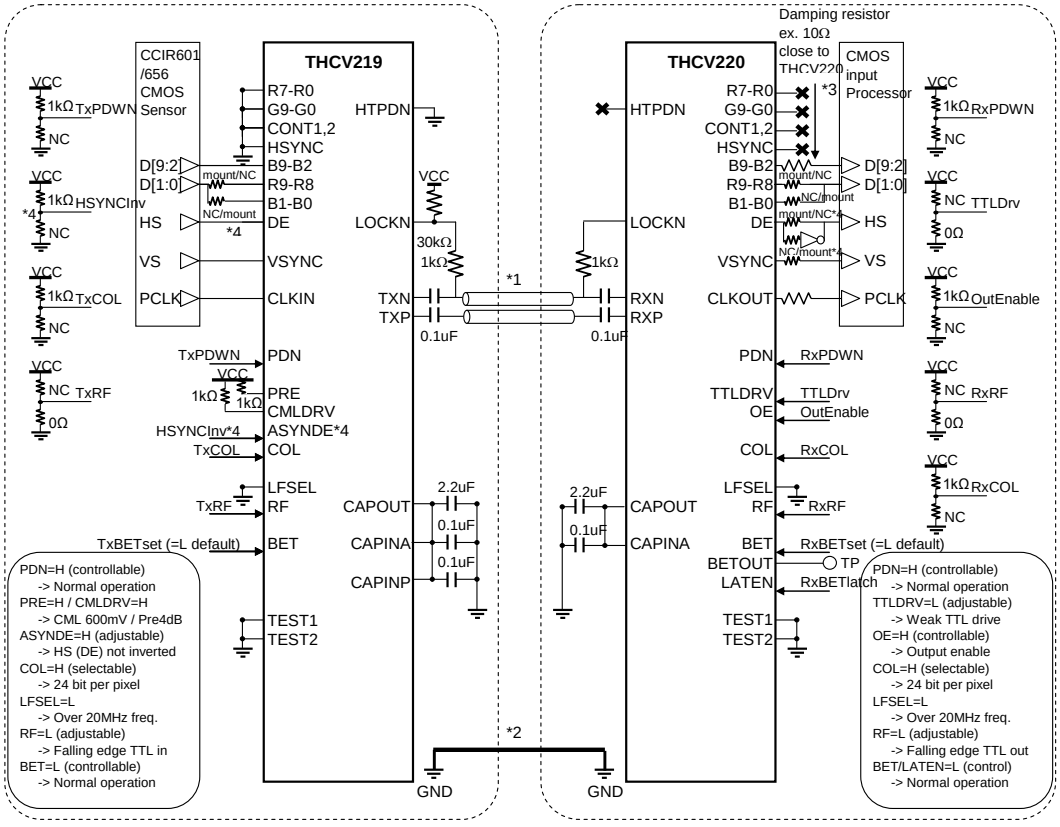
BET pin can be used as Bit Error Test entry in actual configuration in order for debug or test purpose.
Camera HSYNC should be connected to THCV219 DE and polarity must be cared by ASYNDE setting.
[THCV220]
PDN and OE can be controlled by external resistor or other driving source like MCU.
Set COL pin **High** (24bit), LFSEL pin **Low** (over 20MHz) and RF pin properly (Falling or Rising edge).
BET, BETOUT and LATEN pin can be used for Bit Error Test in actual configuration in order for debug or test.
Place 10Ω resistor close to outputs, which can be eliminated when freq. is low, trace is short, and TTLDRV=**L**.
Processor HSYNC should be connected to THCV220 DE and polarity must be cared by external inverter.

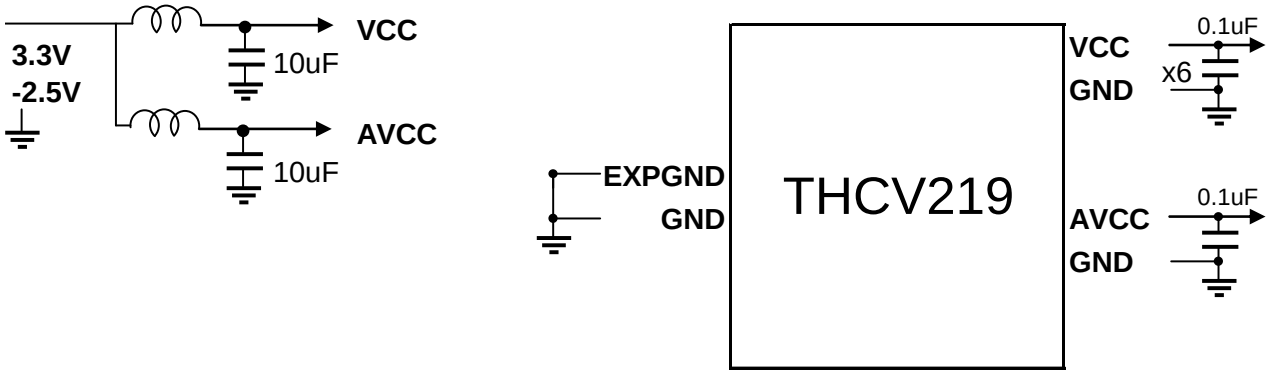


*1 indicates microstrip lines or cables with their differential characteristic impedance being 100Ω
*2 Connect GNDs of both Tx and Rx PCB
*3 TTL output dampling resistor can be totally eliminated if freq. is low and trace is short and TTLDRV=L
*4 System HSYNC signal should be matched to Vx1HS DE requirement. Active image should be during DE=H.

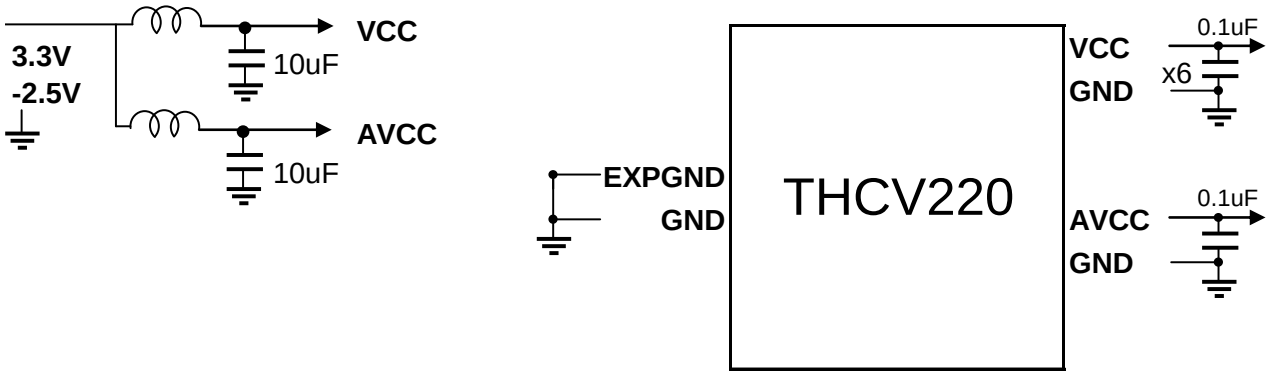
Recommendations for Power Supply

- Separate all the power domains in order to avoid unwanted noise coupling between noisy digital and sensitive analog domains.
- Use high frequency ceramic capacitors of 0.1uF as bypass capacitors between power and ground pins. Place them as close to each power pin as possible. All supply pins need capacitor placement one by one.
- Use the same ground plane for all ground pins including EXPGND.

Recommended Power Supply for THCV219



Recommended Power Supply for THCV220



Note

1)Power On Sequence

Don't input clock nor data before THCV219 is on in order to keep absolute maximum ratings.

2)Cable Connection and Disconnection

Don't connect and disconnect the TLL and CML cable/connector, when the power is supplied to the system.

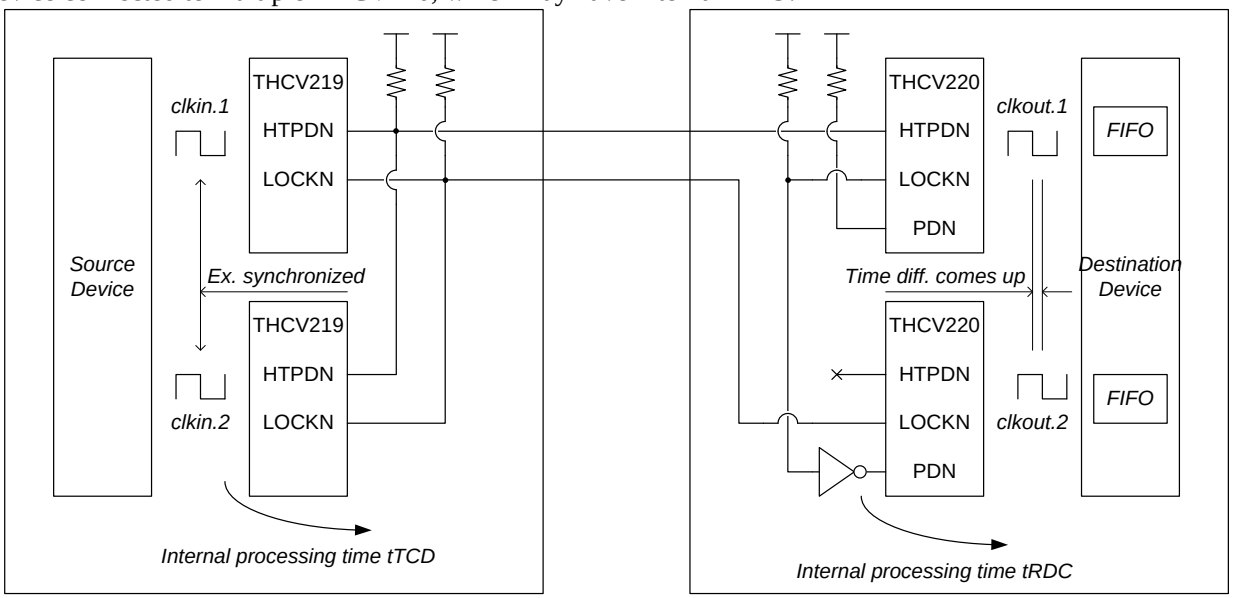
3)GND Connection

Connect the each GND of the PCB where THCV219 and THCV220 are on it. It is better for EMI reduction to place GND cable as close to TTL and CML cable as possible.

4)Multiple device connection

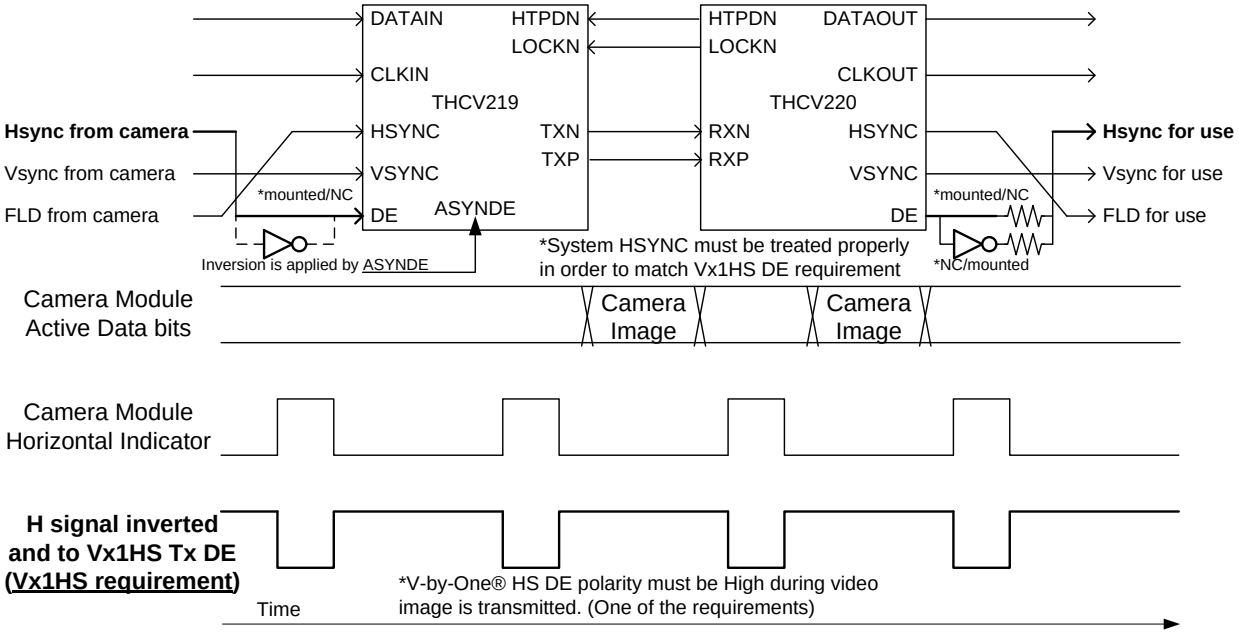
HTPDN and LOCKN signals are supposed to be connected proper for their purpose like the following figure.
HTPDN should be from just one Rx to multiple Tx because its purpose is only ignition of all Tx.
LOCKN should be connected so as to indicate that all Rx CDR become ready to receive normal operation data.
LOCKN of Tx side can be simply split to multiple Tx.
There could be other applicable circuit like 'OR gate of LOCKN', 'npn transistor with resistors as inverter', etc.

Also possible time difference of internal processing time (THCV219 Data sheet p.10 tTCD and THCV220 Data sheet p.11 tRDC) on multiple data stream must be accommodated and compensated by the following destination device connected to multiple THCV220, which may have internal FIFO.

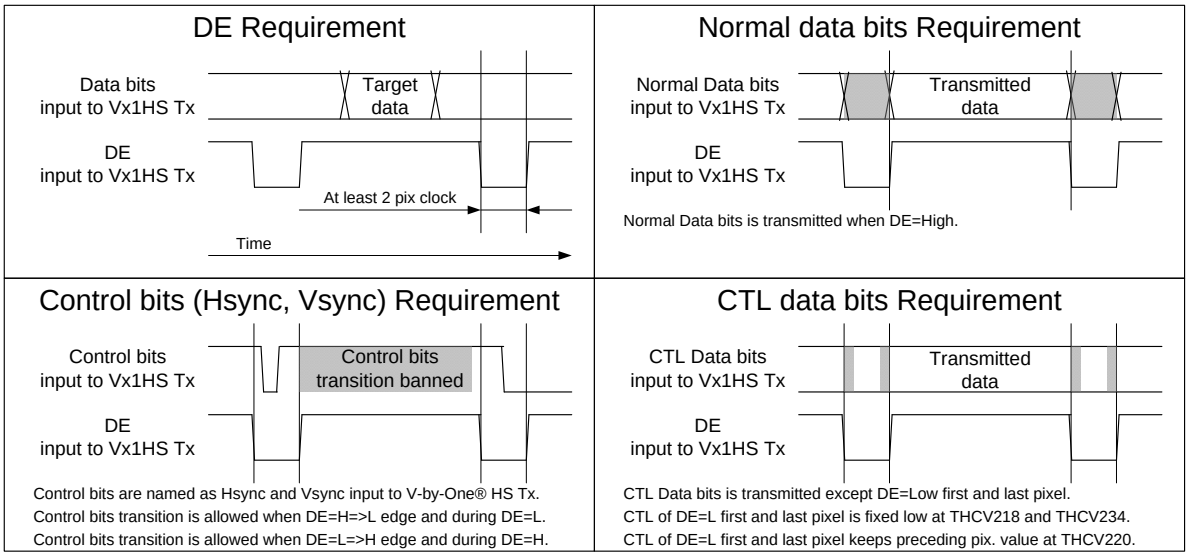


5)In case of No DE in video signal stream

V-by-One® HS transmission always requires DE, while some system has only HSync and VSync.
Sometimes Hsync should be connected to DE and other treatment is at the same time required.
DE polarity on active data transmission period must be High, which sometimes needs external inverter.



Below are consideration points if there is no DE signal on original data format.

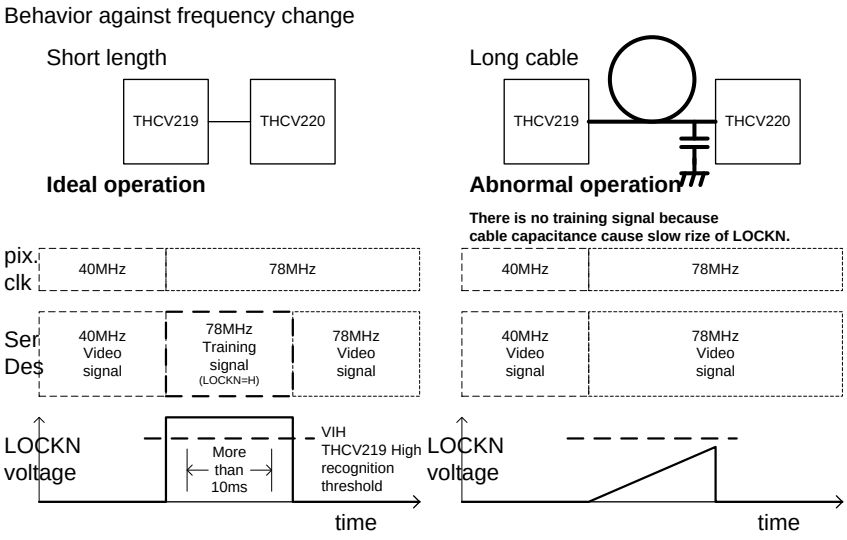


If this kind of configuration is required, please contact to

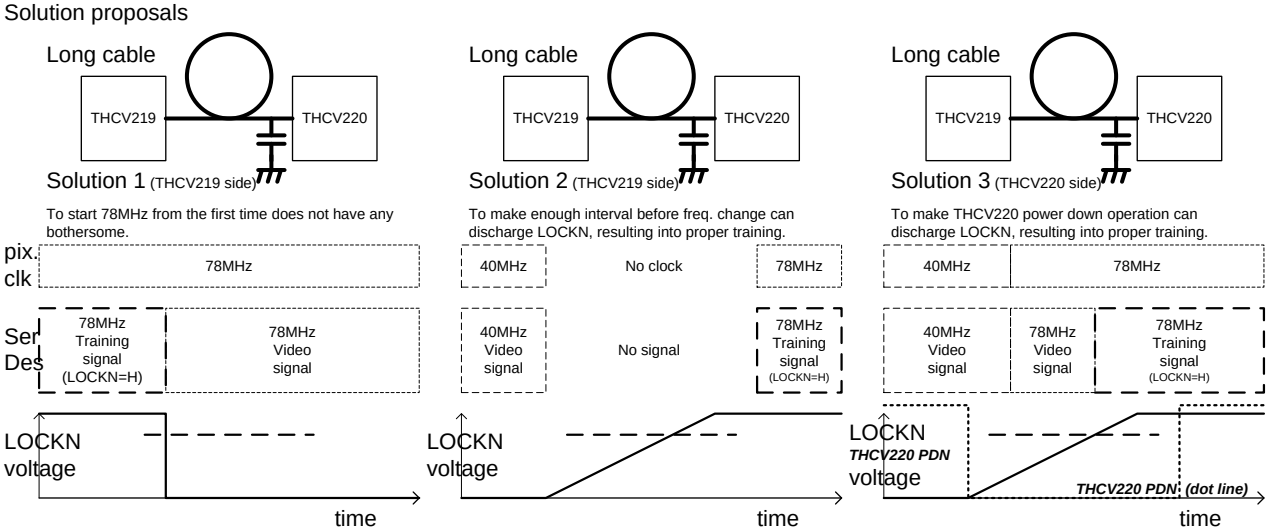
mspsupport@thine.co.jp (for FAE mailing list)

6)In case of long cable over meters transmission with frequency change in operation

Frequency change during operation with long cable may be problematical because long cable has its huge capacitance to slow down LOCKN rise waveform.
LOCKN node must be over VIH at least more than 10ms* for ideal operation.



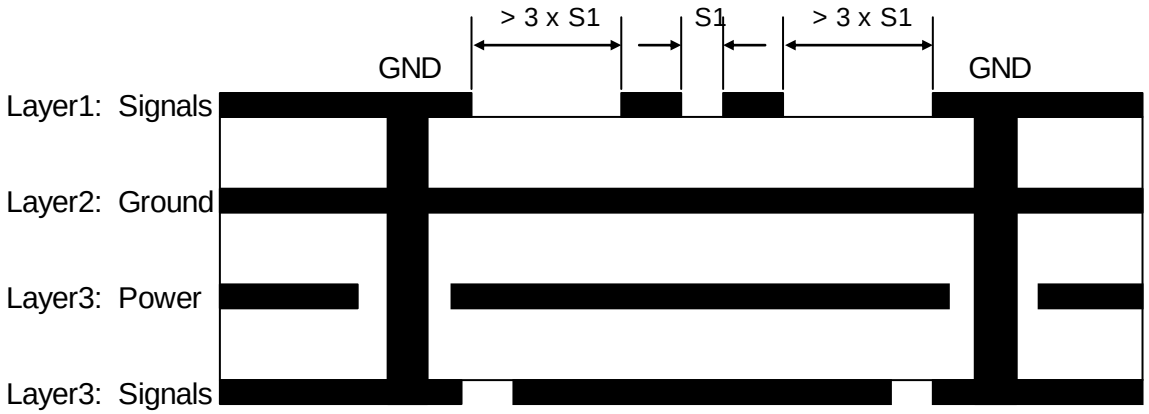
There are 3 available solutions.
Solution1. To start pixel clock as 78MHz from the first time on THCV219 side.
Solution2. To make enough interval before 78MHz to discharge LOCKN up to above VIH on THCV219 side.
Solution3. To make THCV220 power down operation to discharge LOCKN up to above VIH.



PCB Layout Considerations

- Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer. (Refer to figure below.)
- PCB traces for high-speed signals must be single-ended micorstirp lines or coupled microstrip lines whose differential characteristic impedance is 100Ω.
- Minimize the distance between traces of a differential pair (S1) to maximize common mode rejection and coupling effect which works to reduce EMI(Electro-Magnetic Interference).
- Route differential signal traces symmetrically.
- Avoid right-angle turns or minimize the number of vias on the high speed traces because they usually cause impedance discontinuity in the transmission lines and degrade the signal integrity.
- Mismatch among impedances of PCB traces, connectors, or cables also caused reflection, limiting the bandwidth of the high-speed channels.
- Using common-mode filter on differential traces is desirable to reduce EMI. Pay attention on data-rate driven noise. For example, if data-rate is 1.5Gbps, common mode choke coil of 1.5GHz common mode impedance is desired to be high, while 1.5GHz differential impedance is low._

PCB Cross-sectional View
for Microstrip Lines



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2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.

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   5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.
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9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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sales@thine.co.jp